Single Power Supply Synchronous PWM Controller

Description

The NX2155H controller IC is a single input supply synchronous Buck controller IC designed for step down DC to DC converter applications. The NX2155H is optimized to convert bus voltages from 8V to 22V to output as low as 0.8V voltage.

An internal regulator converts the bus voltage to 5V, which provides voltage supply to internal logic and driver circuits. The NX2155H operates at a programmable frequency of 2MHz, and employs loss-less current limiting by sensing the Rdson of synchronous MOSFET followed by hiccup feature. Feedback undervoltage triggers the Hiccup mode.

Other features of the device are: Internal Schottky diode, thermal shutdown, 5V gate drive, adaptive deadband control, internal digital soft start, 5VREG undervoltage lock out and Shutdown capability via the comp pin.

Features

- Single Supply Voltage from 8V to 22V
- Internal 5V Regulator
- Programmable Operational Frequency of 2MHz
- Internal Digital Soft Start Function
- Less than 50nS Adaptive Deadband
- Current Limit Triggers Hiccup by Sensing RDSON of Synchronous MOSFET
- Pb-free and RoHS Compliant

Applications

- LCD TV
- Graphic Card on Board Converters
- Memory Vddq Supply in Mother board Applications
- On board DC to DC such as 12V to 3.3V, 2.5V, or 1.8V
- Hard Disk Drive
- Set Top Box

Typical Application Diagram

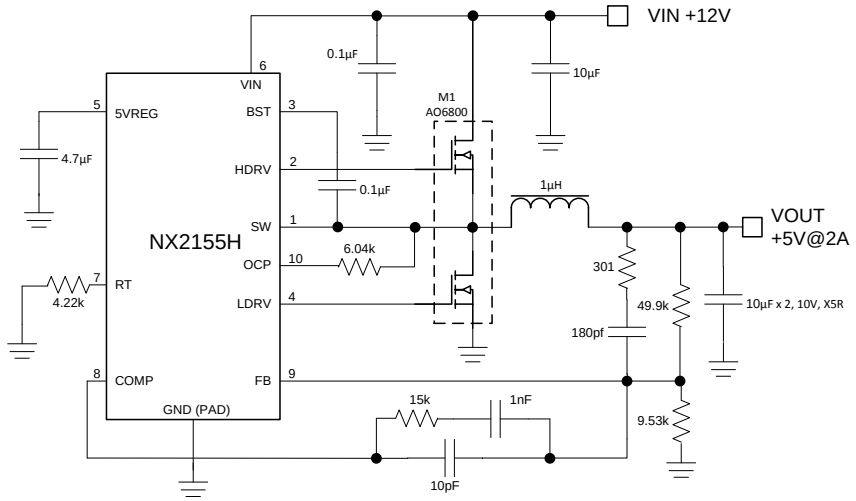


Figure 1 · **Typical Application of NX2155H**

Pin Configuration and Pinout

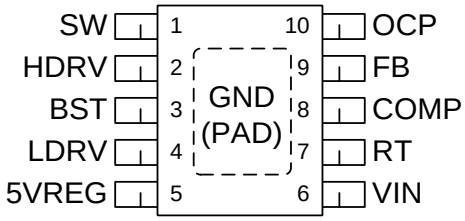


Figure 2 · **Pinout**

Part Marking Line 1 = NX
Line 2 = 115H
Line 3 - YWW
YWW = date code year, week

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 85°C	RoHS compliant, Pb-free	MSOP-EP - 10L	NX2155HIUP	Bulk / Tube
			NX2155HIUP -TR	Tape and Reel

Thermal Properties

Thermal Resistance(θ_{JA})	Type	Units
MSOP 3x3mm 10L exposed pad	46	°C/W

Note: The θ_{Jx} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Pin Description

Pin Number	Pin Designator	Description
1	SW	This pin is connected to the source of the high side MOSFET and provides return path for the high side driver.
2	HDRV	High side MOSFET gate driver.
3	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1µF to1µF must be connected from this pin to SW pin.
4	LDRV	Low side MOSFET gate driver.
5	5VREG	An internal 5V regulator provides supply voltage for the low side fet driver, BST and internal logic circuit. A high frequency 4.7 µF X5R ceramic capacitor must be connected from this pin to the GND pin as close as possible.
6	VIN	Voltage supply for the internal 5V regulator. A high frequency 0.1µF

Pin Number	Pin Designator	Description
		ceramic capacitor must be connected from this pin to GND.
7	RT	Oscillator's frequency can be set by using an external resistor from this pin to GND.
8	COMP	This pin is the output of the error amplifier and together with FB pin is used to compensate the voltage control feedback loop. This pin is also used as a shut down pin. When this pin is pulled below 0.3V, both drivers are turned off and internal soft start is reset.
9	FB	This pin is the error amplifier inverting input. This pin is also connected to the output UVLO comparator. When this pin falls below threshold, both HDRV and LDRV outputs are in hiccup.
10	OCP	This pin is connected to the drain of the external low side MOSFET and is the input of the over current protection (OCP) comparator. An internal current source is flown to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET. Current limit point is this voltage divided by the Rdson.
PAD	GND	This is the ground connection for the power stage of the controller.

Block Diagram

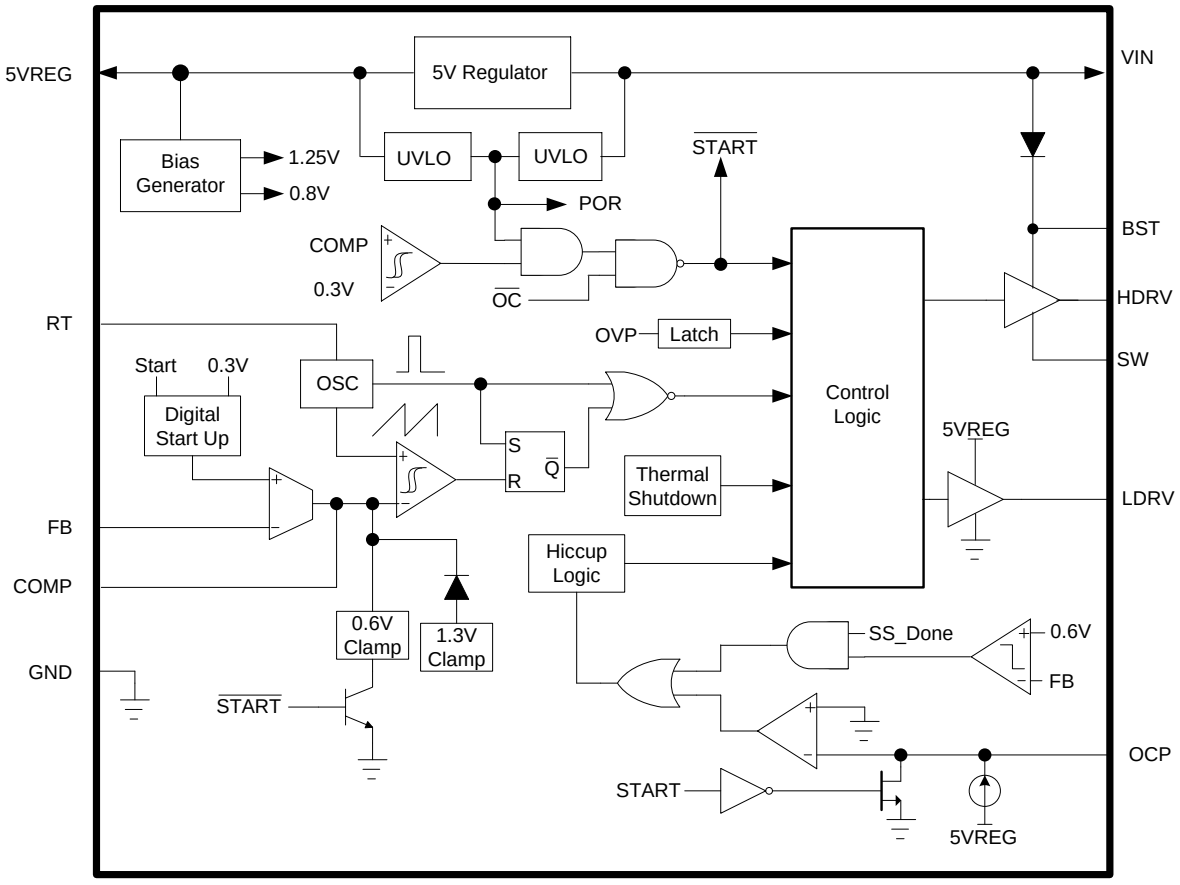


Figure 3 · **Simplified Block Diagram of NX2155H**

Absolute Maximum Ratings

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Parameter	Min	Max	Units
V_{CC} to GND & BST to SW voltage	-0.3	6.5	V
BST to GND Voltage	-0.3	30	V
VIN to GND Voltage	-0.3	25	V
SW to PGND	-2	35	V
All other pins	-0.3	6.5	V
Storage Temperature Range	-65	150	°C
Operating Junction Temperature Range	-40	125	°C
Peak Solder Reflow Temperature		260 (+0, -5)	°C

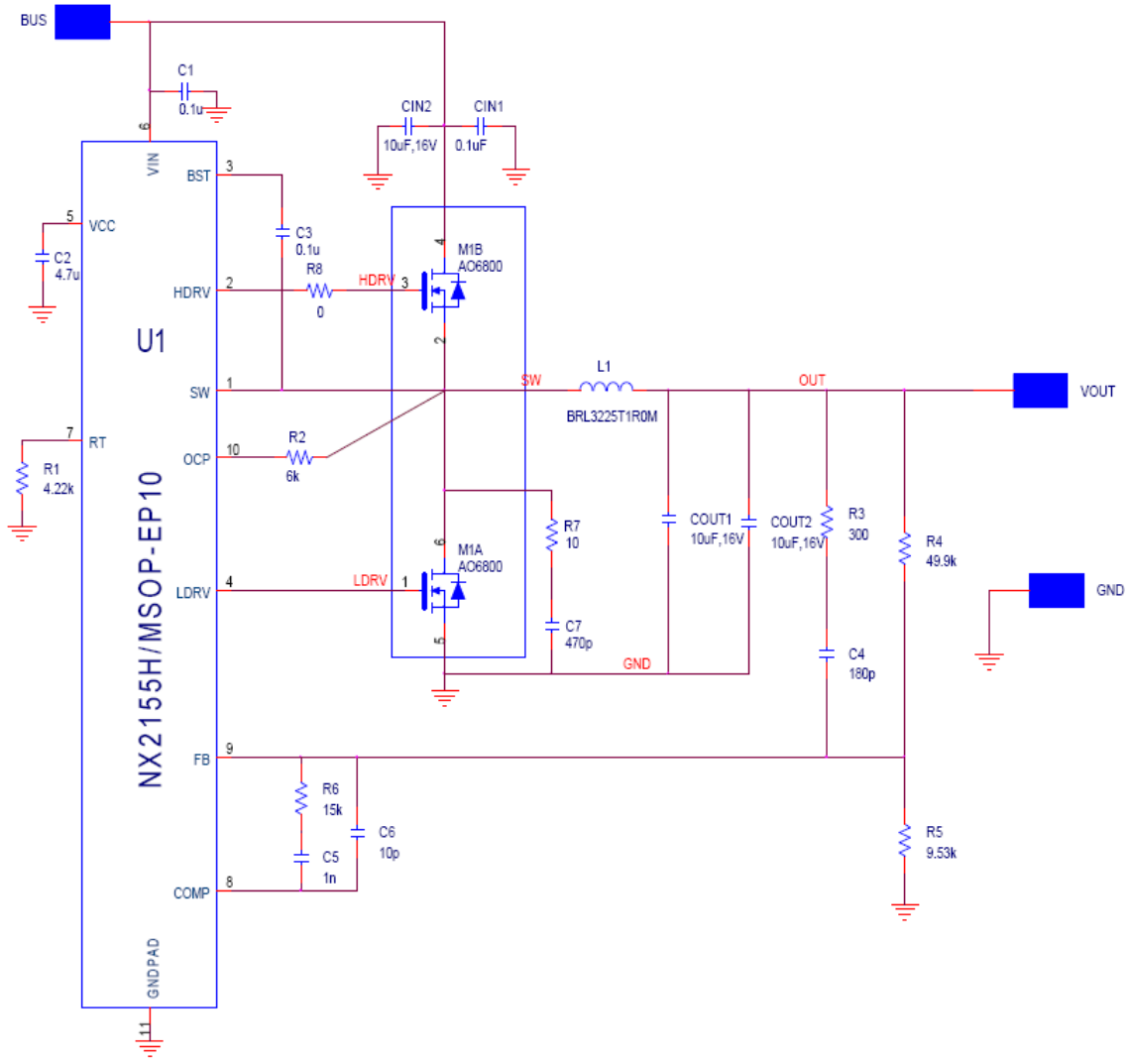
Electrical Characteristics

Unless otherwise specified, these specifications apply over VIN = 12V. and T_A = -40°C to 85°C, with the following bypass capacitors: C_{VIN} = 1µF, C_{5VREG} = 4.7µF, all X5R ceramic capacitors. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage						
V_{REF}	Reference Voltage		0.784	0.8	0.816	V
$V_{REFLINE}$	V_{REF} Line Regulation	VIN = 8V to 22V		0.4		%
FB $_{UVLO}$	Feedback UVLO Threshold		0.54	0.6	0.66	V
5VREG						
5VREG	5VREG Voltage Range		4.875	5.125	5.375	V
$5VREG_{UV}$	5VREG UVLO	5VREG rising		3.76		V
$5VREG_{UVH}$	5VREG UVLO Hysteresis			0.28		V
$5VREG_{REG}$	5VREG Line Regulation	VIN = 9V to 22V		10	20	mV
	5VREG Max Current		20	50		mA
Supply Voltage (VIN)						
VIN	VIN Voltage Range		8		22	V
	Input Voltage Current (Static)	No switching	3.7	4.8	6.5	mA
	Input Voltage Current (Dynamic)	Switching with HDRV and LDRV open @ 2.2MHz	5.4	8	11	mA
VIN_{UV}	VIN UVLO Threshold	VIN rising	6	6.5	7.5	V
VIN_{UVH}	VIN UVLO Hysteresis	VIN falling		0.6		V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Soft Start						
T_{SS}		F_S = 2.2 MHz		580		µS
Oscillator (R_T)						
F_S	Frequency	R_T = 4.22k		2250		kHz
V_{RAMP}	Ramp- Amplitude Voltage		1.15	1.4	1.65	V
	Max Duty Cycle	F_S = 2.2MHz	62	71	80	%
	Min Controllable On Time				150	ns
Error Amplifiers						
	Transconductance		1350	1850	2350	µmho
I_B	Input Bias Current			10		nA
	Comp SD Threshold		0 .14	0.2	0.26	V
High Side Driver (C_L = 2200pf)						
H_{DRVSRC}	Output Impedance, Sourcing	I = 200mA		1.9		Ω
H_{DRVSNK}	Output Impedance, Sinking	I = 200mA		1.7		Ω
$T_{DRVRISE}$	Rise Time			14		ns
$T_{DRVFALL}$	Fall Time			17		ns
$TDRV_{DBAND}$	Dead band Time	L_{DRV} going low to H_{DRV} going high, 10%-10%	7	20	36	ns
Low Side Driver (C_L = 2200pf)						
L_{DRVSRC}	Output Impedance, Sourcing	I = 200mA		1.9		Ω
L_{DRVSNK}	Output Impedance, Sinking	I = 200mA		1		Ω
$T_{DRVRISE}$	Rise Time			25		ns
$T_{DRVFALL}$	Fall Time			25		ns
$TDRV_{DBAND}$	Dead band Time	SW going low to L_{DRV} going high, 10%-10%	30	38	45	ns
OCP						
	OCP Current		30	37	45	µA
Over Temperature Shutdown						
	OTP Threshold			150		°C
	OTP Hysteresis			20		°C
Internal Schottky Diode						
	Forward Voltage Drop	Forward current = 20mA		350	500	mV

Demo Board Design (V_{BUS} = 12V, V_{OUT} = 5V/2A, Frequency = 2.2MHz



* R7 and C7 are optional.

Figure 4 · **Simplified Demo board schematic on NX2155H**

Demoboard Bill of Materials

Item	Quantity	Reference	Part	Manufacturer
1	3	C1,C3,CIN1	0.1µF	
2	1	C2	4.7uF,6.3V,X5R	
3	1	C4	180pF	
4	1	C5	1nF	
5	1	C6	10pF	
6	1	C7	470pF	
7	1	CIN2	10 µF,16V,X5R	
8	2	COUT1,COUT2	10 µF,10V,X5R	
9	1	L1	BRL3225T1R0M	Taiyo Yuden
10	1	M1	AO6800	AOS
11	1	R1	4.22kΩ	
12	1	R2	6kΩ	
13	1	R3	300Ω	
14	1	R4	49.9kΩ	
15	1	R5	9.53kΩ	
16	1	R6	15kΩ	
17	1	R7	10Ω	
18	1	R8	0Ω	
19	1	U1	NX2155H/MSOP-EP10	Microsemi -AMSG

Demo Board Waveforms

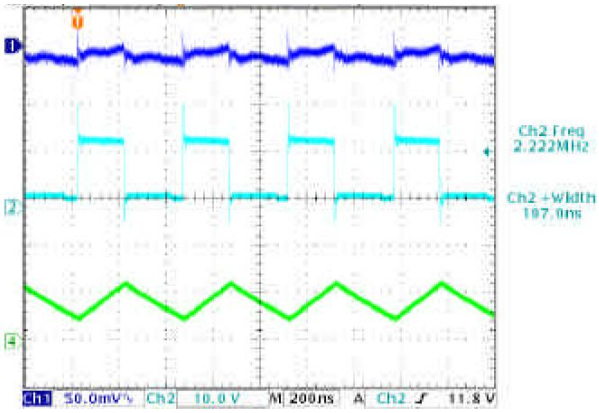


Figure 5 · Output Ripple (CH1 V_{OUT} AC 50mV/Div, CH2 SW 10V/Div, CH4 Output Current 2A/Div)

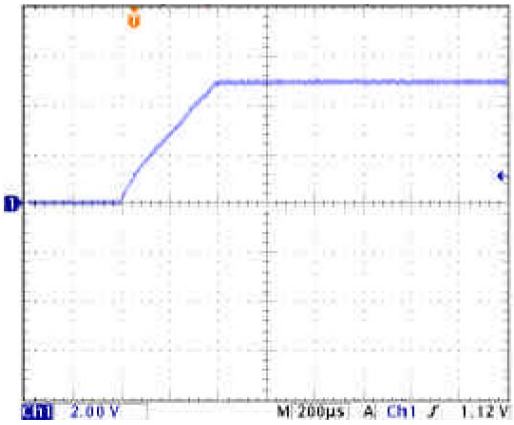


Figure 6 · Startup (Ch1 VOUT 2V/Div)

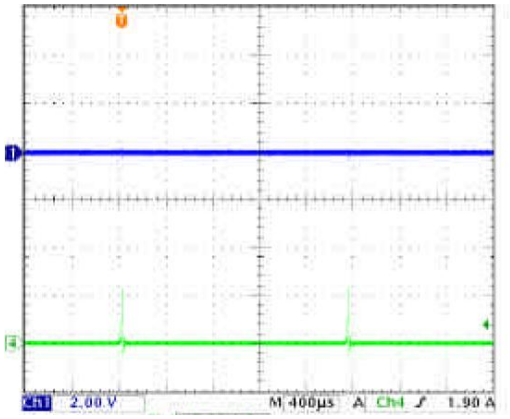


Figure 7 · OCP Protection during output short (CH1 V_{OUT} 2V/Div, CH4 Output Current 5A/Div)

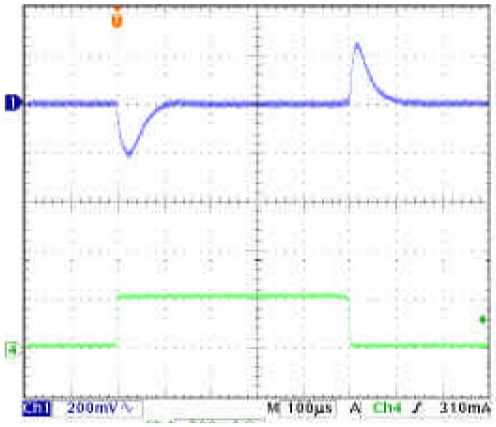


Figure 8 · Output Dynamic Response(CH1 V_{OUT} AC 200mV/Div, , CH4 Output Current 500mA/Div)

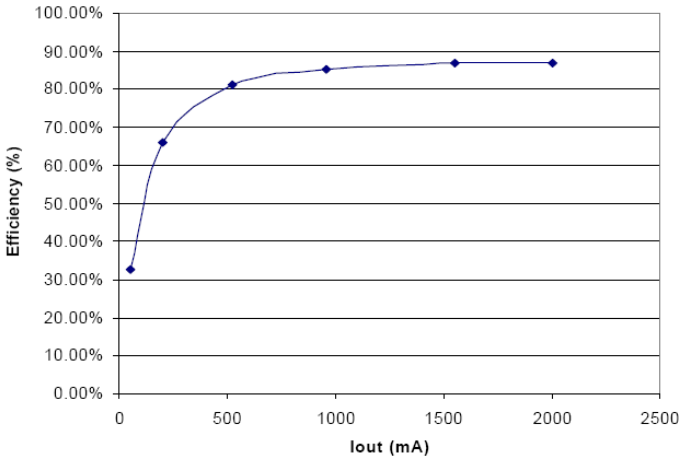


Figure 9 · **Output Efficiency**

Demo Board Layout

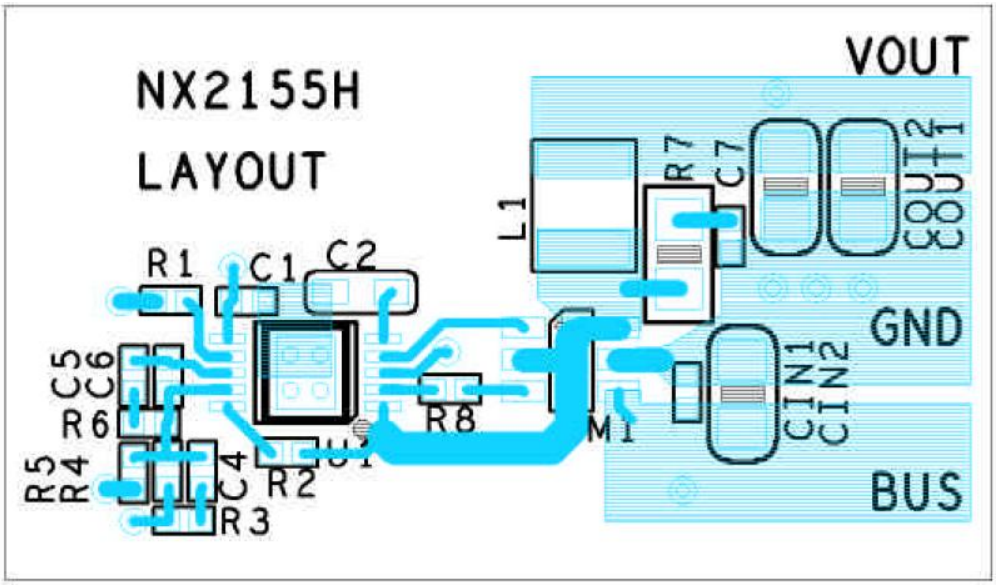


Figure 10 · **Top Layer**

Figure 11 · **Ground Layer**

Demo Board Layout

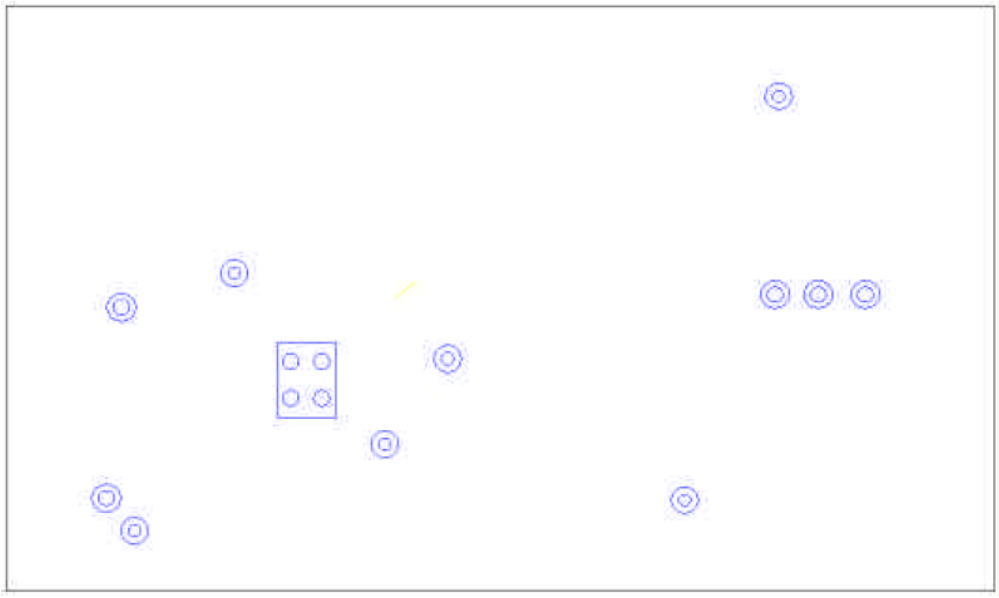


Figure 12 · **Power Layer**

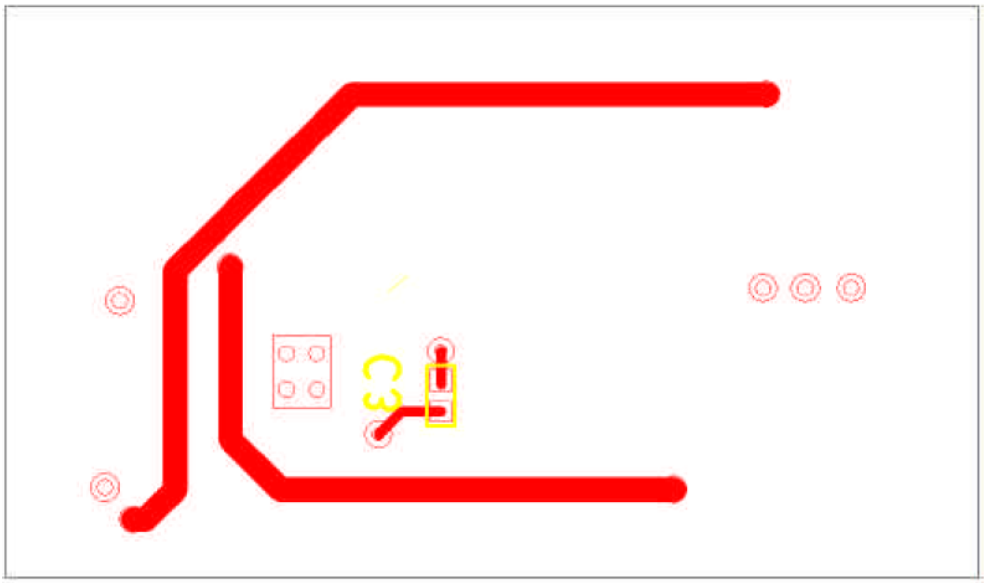


Figure 13 · **Bottom Layer**

Demo Board Design (V_{BUS} = 12V, V_{OUT} = 5V/10A, Frequency = 400kHz

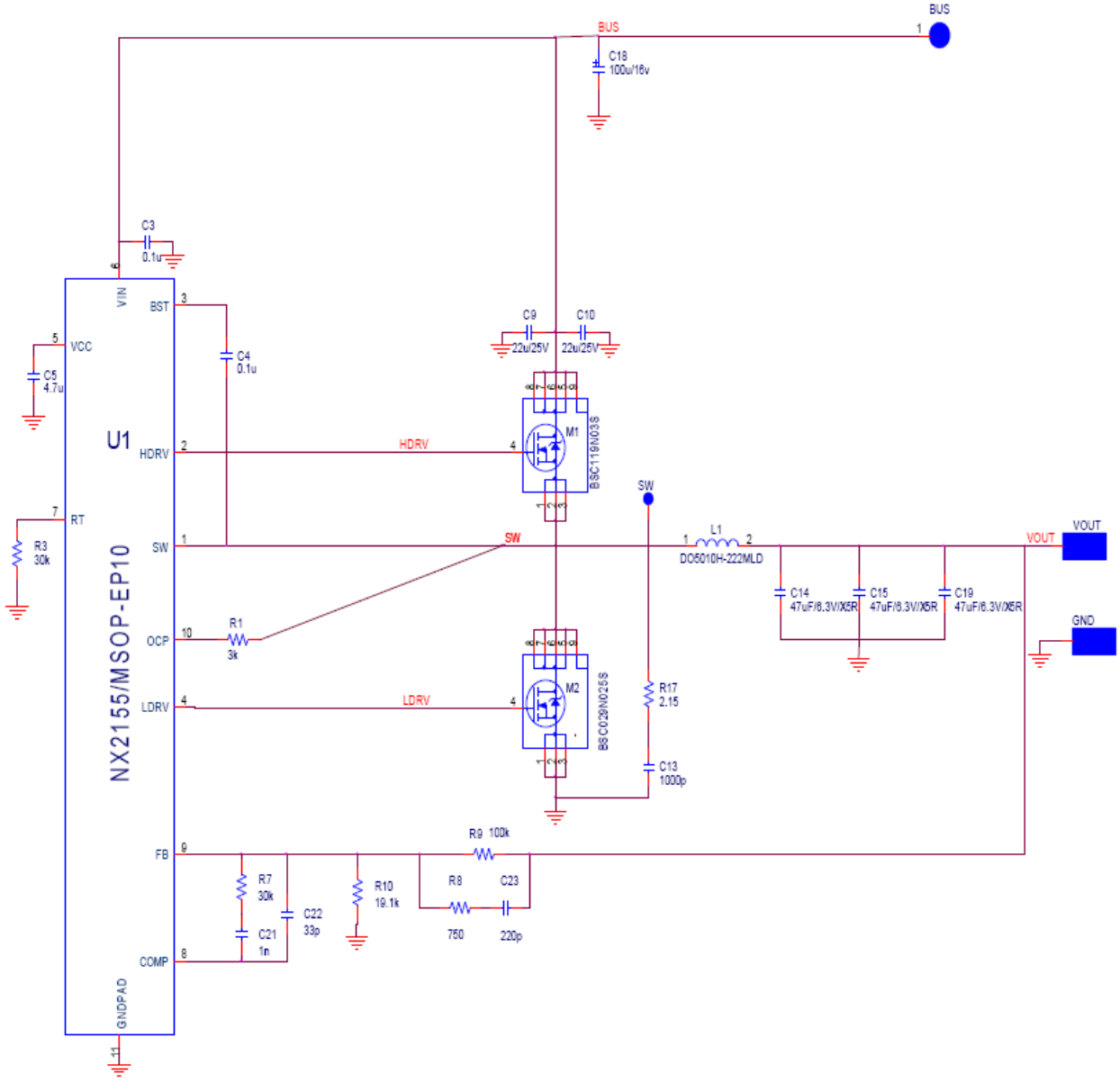


Figure 14 · **Simplified Demo board schematic on NX2155H**

Item	Quantity	Reference	Part	Manufacturer
1	2	C3,C4	0.1µF	
2	1	C5	4.7µF	
3	2	C9,C10	22µF,25V,X5R	
4	1	C13	1000pF	
5	3	C14, C15, C19	4.7µF,6.3V,X5R p	
6	1	C18	100µF,16V	
7	1	C21	1nF	
8	1	C22	33pF	
9	1	C23	220pF	
10	1	L1	DO5010H-222MLD	Coilcraft
11	1	M1	BSC119N03S	Infineon
12		M2	BSC029N025S	Infineon
13	1	R1	3.0kΩ	
14	2	R3, R7	30kΩ	
15	1	R8	750Ω	
16	1	R9	100kΩ	
17	1	R10	19.1kΩ	
18	1	R17	2.15Ω	
19	1	U1	NX2155H/MSOP-EP10	Microsemi -AMSG

Demo Board Waveforms

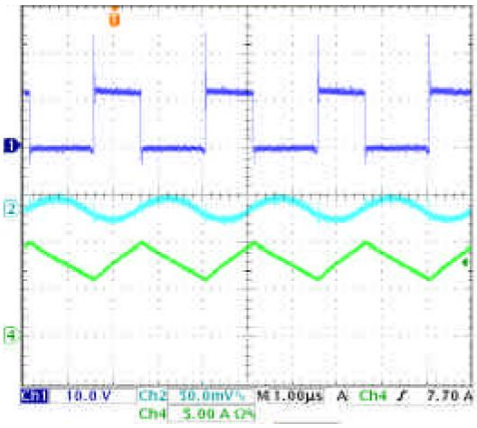


Figure 15 · Output Ripple (CH1 SW 10V/Div, CH2 VOUT AC 50mV/Div, CH4 Output Current 5A/Div)

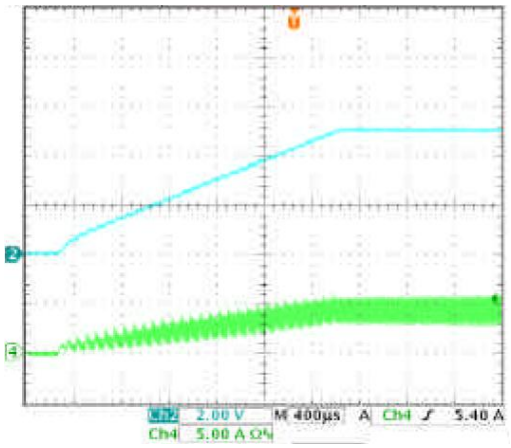


Figure 16 · Startup (Ch1 VOUT 2V/Div, Ch4 Inductor Current 5A/Div)

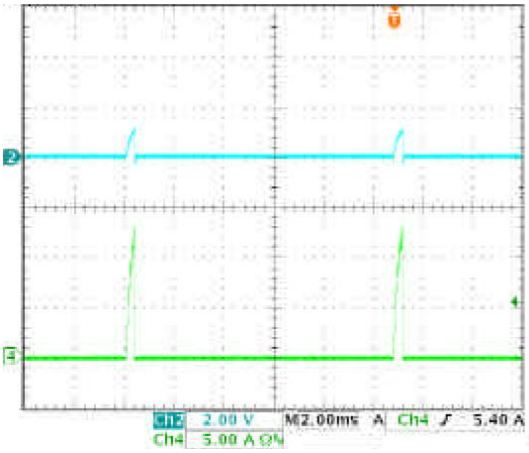


Figure 17 · OCP Protection during short (CH2 V_{OUT} 2V/Div, CH4 Output Current 5A/Div)

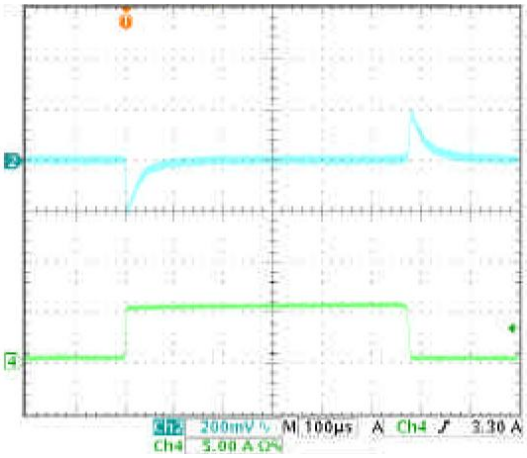


Figure 18 · Output Dynamic Response(CH1 V_{OUT} AC 200mV/Div, , CH4 Output Current 5A/Div)

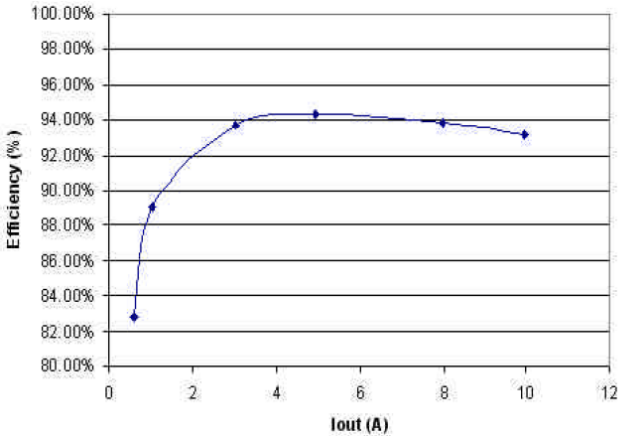


Figure 19 · **Output Efficiency**

Application Information

Symbol Used In Application Information:

Symbol	Description
V_{IN}	Input voltage
V_{OUT}	Output voltage
I_{OUT}	Output current
ΔV_{RIPPLE}	Output voltage ripple
F_S	Working frequency
ΔI_{RIPPLE}	Inductor current ripple

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT} = \frac{V_{IN} \times V_{OUT}}{\Delta I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_S}$$

$$\Delta I_{RIPPLE} = K \times \frac{I_{OUTPUT}}{N}$$

where k is between 0.2 to 0.4.

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state (DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both conditions. The amount of voltage ripple during the DC load condition is determined by the following equation:

$$\Delta V_{RIPPLE} = ESR \times \Delta I_{RIPPLE} + \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

Where ESR is the output capacitors' equivalent series resistance, C_{OUT} is the value of output capacitors. Typically when ceramic capacitors are selected as output capacitors, DC ripple spec is easy to be met, but multiple ceramic capacitors are required at the output to meet transient requirement.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift, and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin. Ideally, the Bode plot of the closed loop system has crossover frequency between 1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with 20dB/decade.

Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the

zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III Compensator Design

For low ESR output capacitors, typically such as Sanyo Os-Con and Poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator.

The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2 \times \pi \times R_4 \times C_2}$$

$$F_{Z2} = \frac{1}{2 \times \pi \times (R_2 + R_3) \times C_3}$$

$$F_{P1} = \frac{1}{2 \times \pi \times R_3 \times C_3}$$

$$F_{P2} = \frac{1}{2 \times \pi \times R_4 \times \frac{C_1 \times C_2}{C_1 + C_2}}$$

Where, F_{Z1}, F_{Z2}, F_{P1}, and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 10. The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1 - g_m \times Z_f}{1 + g_m \times Z_{in} + Z_{in}/R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: R_4>>2/gm. And it would be desirable if $R_1||R_2||R_3$>>1/gm can be met at the same time.

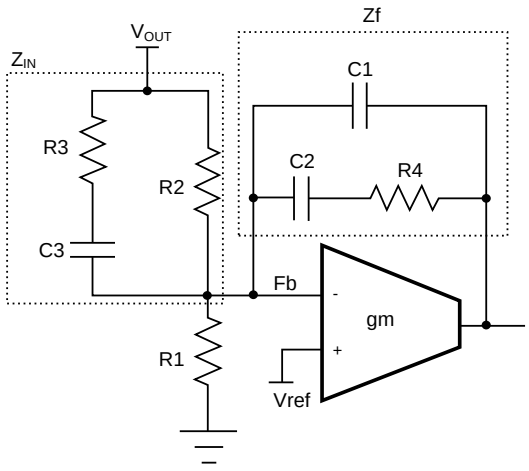


Figure 20 · **Type III Compensator using Transconductance Amplifier**

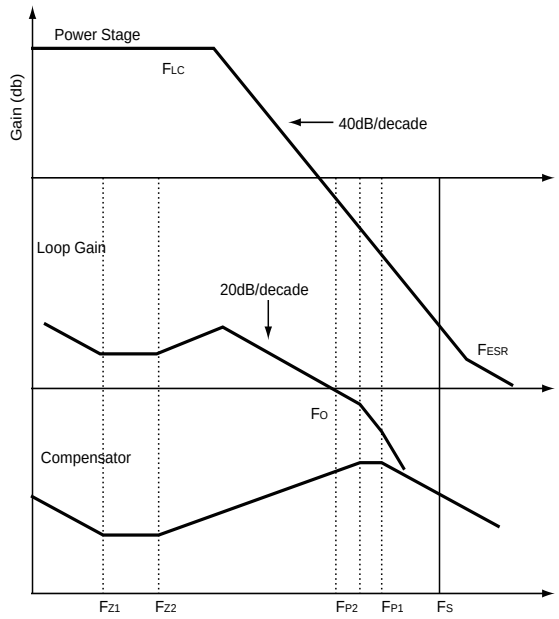


Figure 21 · **Bode Plot of Type III Compensator**

B. Type II Compensator Design

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 12. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain = g_m \times \frac{R_1}{R_1 + R_2} \times R_3$$

$$F_Z = \frac{1}{2 \times \pi \times R_3 \times C_1}$$

$$F_P \approx \frac{1}{2 \times \pi \times R_3 \times C_2}$$

For this type of compensator, FO has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10~1/5F_s$.

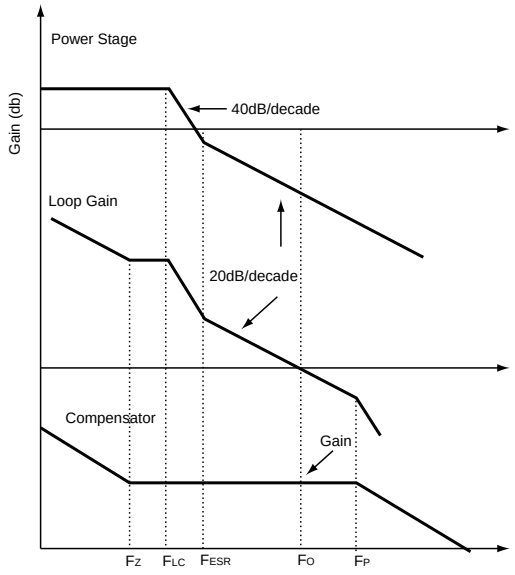


Figure 22 · **Bode Plot of Type II Compensator**

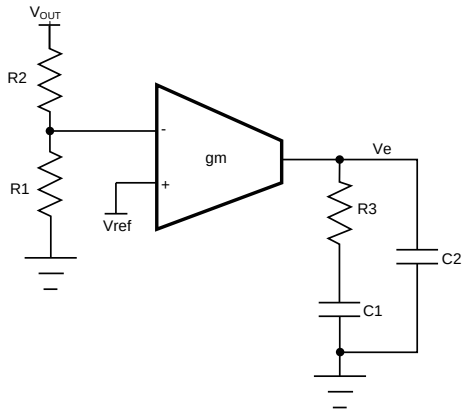


Figure 23 · **Type II Compensator with Transconductance Amplifier**

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT}, V_{REF}, and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}}$$

Where, R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider. See compensator design for R_1 and R_2 selection.

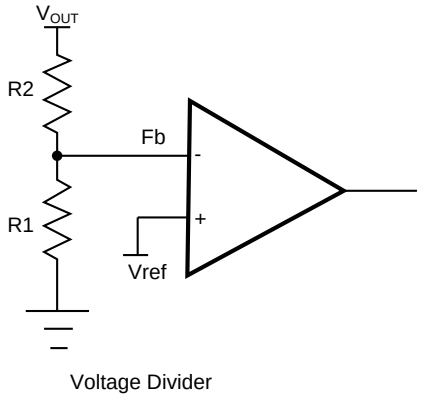


Figure 24 · **Voltage Divider**

Over Current Protection

Over current protection is achieved by sensing current through the low side MOSFET. A typical internal current source of 37µA flowing through an external resistor connected from OCP pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW} = -I_L \times R_{DSON}$$

The voltage at pin OCP is given as

$$I_{OCP} \times R_{OCP} + V_{SW}$$

When the voltage is below zero, the over current occurs.

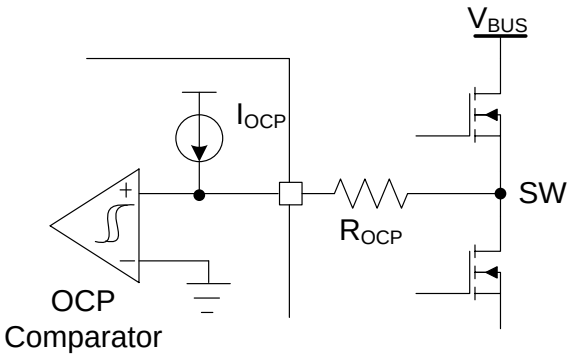


Figure 25 · **Over Current Protection**

The over current limit can be set by the following equation

$$I_{SET} = \frac{I_{OCP} \times R_{OCP}}{K \times R_{DSON}}$$

Frequency Selection

The frequency can be set by external RT resistor. The relationship between frequency and RT pin is shown as follows:

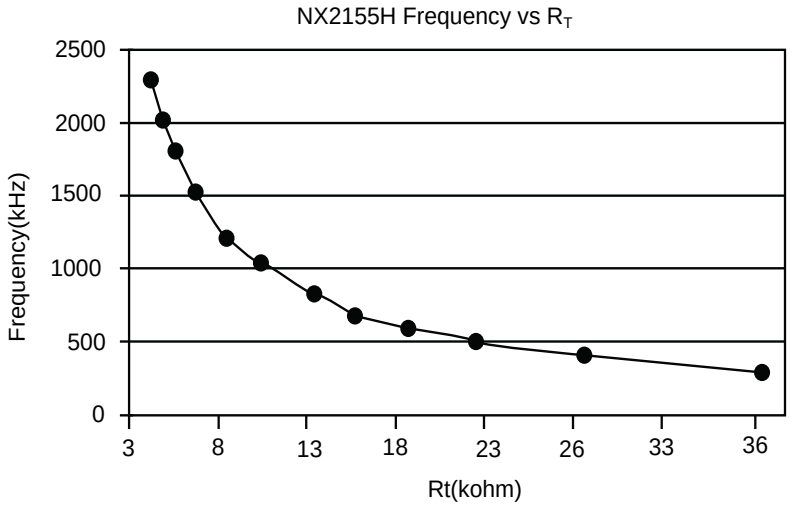


Figure 26 · **Frequency Versus R_T Resistor**

MSOP 10 Pin With Exposed Pad Package Outline Dimensions

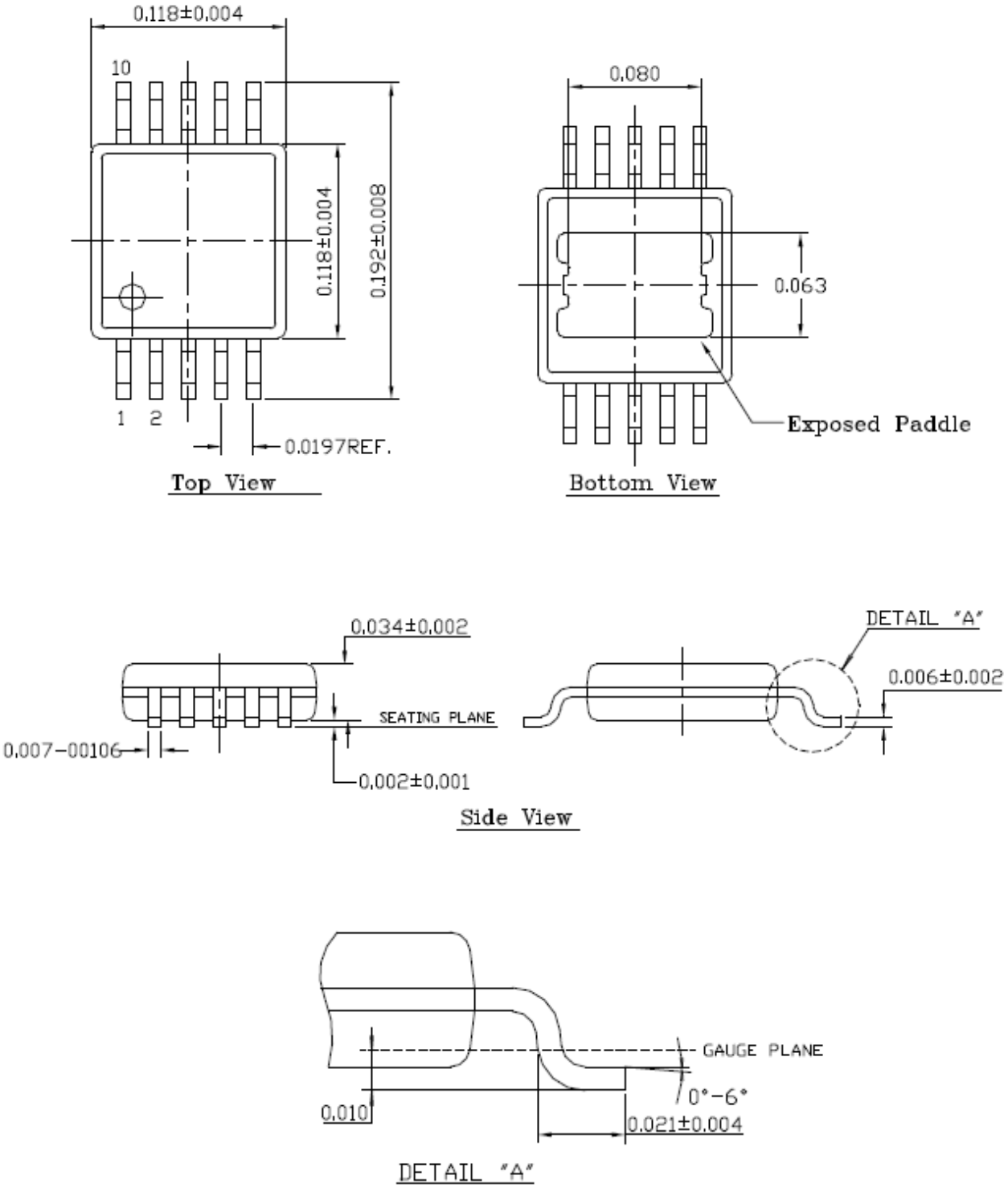


Figure 27 · **Package Outline Dimensions**

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