SINGLE CHIP TRANSCEIVER FOR WALKIE TALKIE

Rev.0.1–Aug.2011

1. General Description

The RDA1846S is a highly integrated single-chip transceiver for Walkie Talkie applications. It totally realizes the translation from RF carrier to voice in the RX path and from voice to RF carrier in the TX path, requiring only one micro controller.

The RDA1846S has a powerful digital signal processor, which makes it have optimum voice quality, flexible function options, and robust performance under varying reception conditions.

The RDA1846S can be tuned to the worldwide frequency band for Walkie Talkie from 400MHz to 500MHz and especially from 134MHz to 174MHz which meets the frequency band of weather broadcast.

The transceiver uses the CMOS process with a package size of 5X5mm. By virtue of its high integration, it requires the least external components and eliminates the complicated design of sensitive RF circuits on PCB.

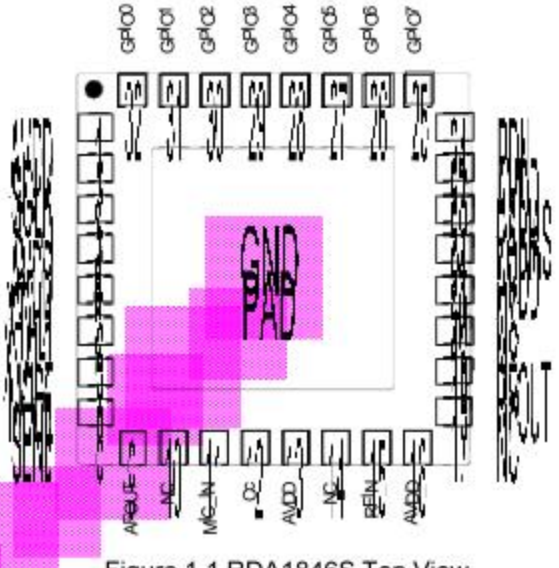


Figure 1.1 RDA1846S Top View

1.1 Features

- CMOS single-chip fully-integrated transceiver
- Fully integrated frequency synthesizer and VCO
- Support worldwide frequency band
  - RDA1846S :134MHz ~ 174MHz
    200MHz~ 260MHz
    400MHz ~ 520MHz
- 12.5KHz, 25KHz channels
- Support multiple XTAL clocks
  - 12.8/25.6Mhz
  - 13/26Mhz
- Digital auto frequency control (AFC)
- Digital auto gain control (AGC)
- Selectable pre/de-emphasis
- Received signal strength indicator (RSSI)
- VOX and SQ
- Build-in CTCSS/CDCSS generator and judgment
  - CTCSS with 120/180 /240 degree phase shift
  - 23/24 bit programmable DCS code
- DTMF and programmable in-band dual tone
- Programmable in-band single tone transmitter
- Auto RX/TX/SLEEP state switching
- 8 GPIOs
- 3-wire/4-wire/I ^{2}C serial control bus interface
- On chip 8 dBm PA
- Analog and digital volume control
- Directly support 32Ω resistance loading
- 3.3 to 4.8 V supply voltage with Integrated LDO
- 5X5 mm 32 pin QFN package

1.2 Applications

- Cellular handsets
- Family radio services
- Walkie Talkies

2. Table of Contents

3. Functional Description

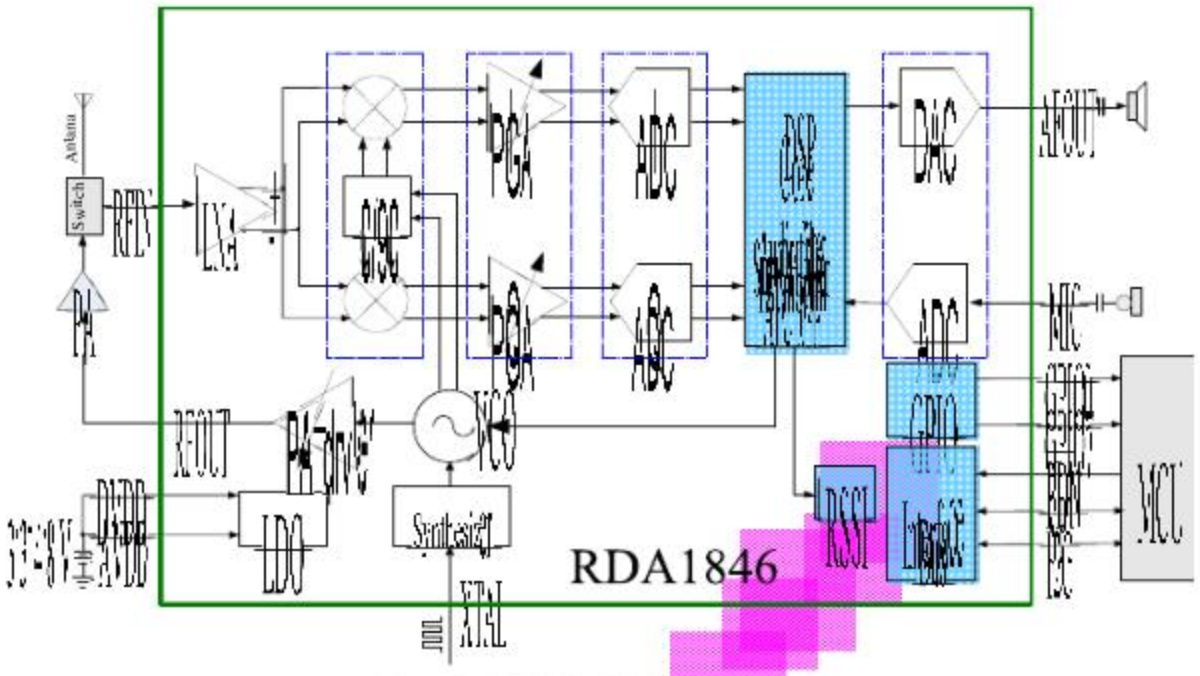


Figure 3.1 RDA1846S Block Diagram

The RDA1846S transceiver features very low solution cost and reduced complexity. As shown in Fig.3.1, to totally complete the translation from RF carrier to voice in the RX path and from voice to RF carrier in the TX path, the chip integrates nearly all the functional blocks including RF and base band analog blocks and digital signal processor. It requires only one micro controller and a few external components to realize a walkie-talkie.

A powerful integrated DSP accomplishes both the demodulation and modulation of the FM signal. Besides, standard walkie-talkie features such as CTS, CDS, VOX and SQ etc. are provided through the 8 GPIOs of the chip. Especially, by virtue of the state-of-the-art CMOS technology advanced algorithms such as AFC, AGC, RSSI and SNR calculations are realized in the DSP , which guarantees the high receiving and transmitting quality while still consumes a low power. Flexible RX/TX/SLEEP auto switching function from the DSP further reduces the average power consumptions.

LDOs are also integrated in the chip which further reduces the BOMs.

All interface pins of the chip will be shortly explained below. For details, refer to the 'RDA 1846 programming guide'.

3.1 RF input and output

The chip can receive and transmit RF signals from 400 to 500MHz and from 134 to 174MHz which cover most of the walkie-talkie frequency bands around the world and the weather broadcast band. For the RF input, a direct-in connection from the antenna to the LNA input pin through a switch is suggested which means no input impedance matching is needed for the receive band. For the RF out, a pa diver can deliver no more than 8 dBm power to PA. PA bias voltage from 1.5V~2.8V for the power amplifier can be supplied from the PABIAS pin.

3.2 Voice input and output

In the RX path, the voice signal after demodulation is sent to the internal DAC which can directly drive a 32Ω resistance loading through AC coupling. In the TX path, microphone signal can be sent into the chip through AC coupling capacitors.

3.3 Synthesizer

The frequency synthesizer generates the local oscillator signal. All building blocks are fully integrated without any external components. LO frequency can be programmed through the serial interface by the MCU. *(How to select frequency band and program LO frequency, refer to the programming guide)*

3.4 XTAL Clock

The RDA1846S supports XTAL clocks such as 12.8 MHz, 13 MHz, 25.6 MHz and 26 MHz. The internal XTAL oscillator can also be bypassed thus TCXO clock with appropriate amplitude can be sent into the chip directly. *(How to configure the internal XTAL oscillator, refer to the programming guide)*

3.5 DSP functions

The DSP accomplishes the demodulation and modulation of the FM signal. Standard walkie-talkie features such as CTS, CDS, VOX and SQ etc. are provided through the 8 GPIOs. *(How to configure the GPIOs, refer to the programming guide)*

3.6 Integrated LDO

LDOs are integrated on chip which eliminates using one LDO chip on the PCB. Supply voltage for the chip is suggested to be within 3.3V~4.8V. A common share of the supply voltage for RDA1846S and other chips or on board circuits are not appropriate and thus not recommended.

3.7 Serial Control Interface

A 3-wire/4-wire/I^2C serial interface is provided for host IC to read and write RDA1846S control registers. *(For details of the serial control interface, refer to the programming guide)*.

4. Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
AVDD	Supply Voltage from battery or LDO	3.3	3.3	4.8	V
T_{amb}	Ambient Temperature	-25	27	+85	℃
V_L	CMOS Low Level Input/output Voltage	0		0.3	V
V_H	CMOS High Level Input/output Voltage	2.7		3	V
V_{TH}	CMOS Threshold Voltage	1.5			V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	-40		+90	°C
I_{IN}	Input Current	-10		+10	mA
V_{IN}	Input Voltage	-0.3		3.3	V
V_{lna}	LNA Input Level			+10	dBm

Table 4-3 Power consumption specification

(AVDD = 3.3 V, T_A = -25 to 85℃, unless otherwise specified)

STATE	DESCRIPTION	Condition	TYP	UNIT
I_{Rx}	Continue Receive	RXON=1,PDN=1	58	mA
I_{Tx}	Continue Transmit	TXON=1,PDN=1	50	mA
I_{sleep}	Deep sleep	PDN=0	60	μA

5. Receiver/Transmitter Characteristics

Table 5-1 Receiver Characteristics

(AVDD = 3.3 V, TA = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
Fin	Input Frequency Range1	RDA1846S	400		520	MHz
	Input Frequency Range2	RDA1846S	134		174	MHz
	Input Frequency Range3	RDA1846S	200		260	MHz
NF	Noise Figure	Max RX Gain		3		dB
$IP3_{in}$	Input IP3	Max RX Gain	-10	-6	0	dBm
SEN	Sensitivity	12.5kHz channel, 12dB SINAD	-125	-124	-123	dBm
ACS	Adjacent Channel Selectivity	±12.5KHz	64	65	69	dB
IR	Image rejection		60	70		dB
	Blocker >	1MHz		85		dB
	Voice distortion		2.0	2.1	2.5	%

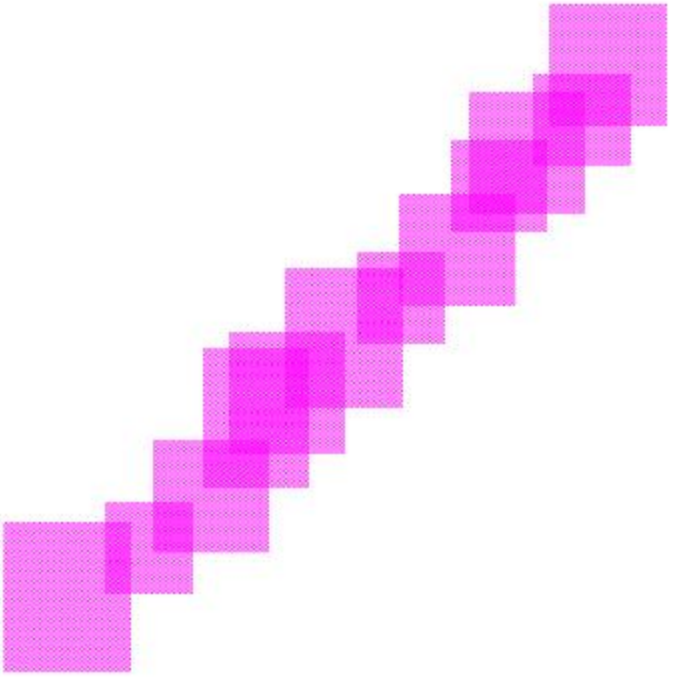
Table 5-2 Transmit Characteristics

(AVDD = 3.3 V, TA = -25 to 85°C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
Fout	Output Frequency Range1	RDA1846S	400		520	MHz
	Output Frequency Range2	RDA1846S	134		174	MHz
	Output Frequency Range3	RDA1846S	200		260	MHz
POUT	Output Power		-12	7	7.5	dBm
SINAD/SNR				45/53		dB
ACP	Adjacent channel power		-61	-64	-67	dBc
	Modulation sensitivity	1.5kHz frequency offset	10	11	12	mV
	Voice distortion		0.4	0.5	0.6	%
	Modulation limitation			2.2	2.5	kHz

6. Control Interface Characteristics

Refer to the 'RDA1846S programming guide'.



7. Pins Description

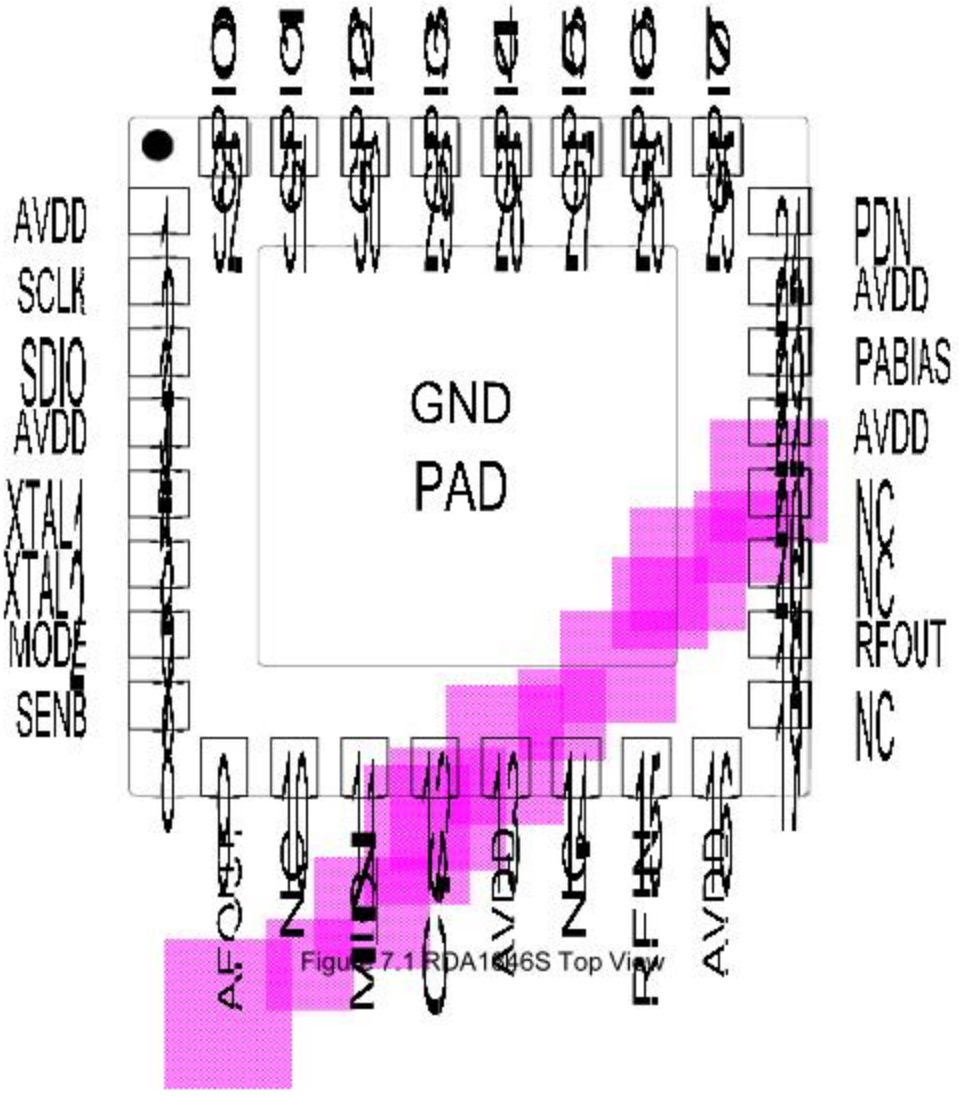


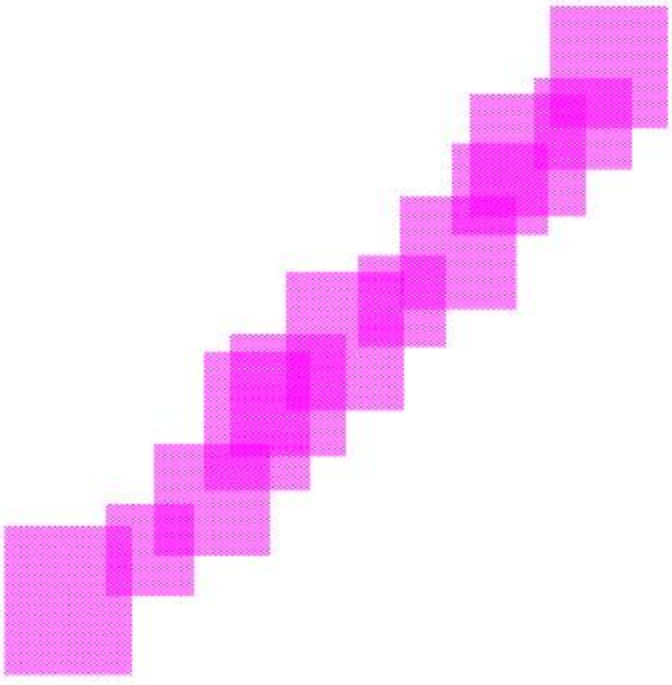
Figure 7.1 RDA1846S Top View

Table 7-1 RDA1846S Pins Description

SYMBOL	PIN	DESCRIPTION
AVDD 1		Power supply
SCLK	2	Clock input for serial control bus
SDIO	3	Data input/output for serial control bus
AVDD 4		Power supply
XTAL1	5	Oscillator pin 1
XTAL2	6	Oscillator pin 2
MODE 7		Control Interface select When MODE = V_L, I^2C Interface is select When MODE = V_H, SPI Interface is select
SENB	8	Latch enable (active low) input for serial control bus
AFOUT	9	Audio signal output to speaker
NC* 10		No connection
MIC_IN 11		MIC input
Cc	12	Compensation capacitor connection pin
AVDD 13		Power supply
NC* 14		No connection
RFIN	15	RF signal input
AVDD 16		Power supply
NC* 17		No connection
RFOUT	18	RF signal output
NC* 19		No connection
NC* 20		No connection
AVDD 21		Power supply
PABIAS	22	PA bias supply for PA
AVDD 23		Power supply
PDN 24		Chip enable, high active Chip sleep , low active
GPIO7 25		Gpio7 / vox (When Gpio7=V_H, vox is active; else V_L)
GPIO6 26		Gpio6 / sq (When Gpio6=V_H, sq is active; else V_L)
GPIO5 27		Gpio5 / txon (When Gpio5=V_H, txon is active; else V_L)
GPIO4 28		Gpio4 / rxon (When Gpio4=V_H, rxon is active; else V_L)
GPIO3 29		Gpio3 / sdo (Gpio3=V_H or V_L, it is the output register data in 4 wire control interface mode)
GPIO2	30	Gpio2 / int

		(When Gpio2=V_H, int is active; else V_L)
GPIO1 31		Gpio1 / code_in / code_out (Gpio1=V_H or V_L, it is the input/output code data)
GPIO0 32		Gpio0 / css_in / css_out (Gpio0=V_H or V_L, it is the input/output CTCSS/CDCSS signal)

***Attention: all NC pins should be floating. Do not connect it to GND!**



8. Application Diagram

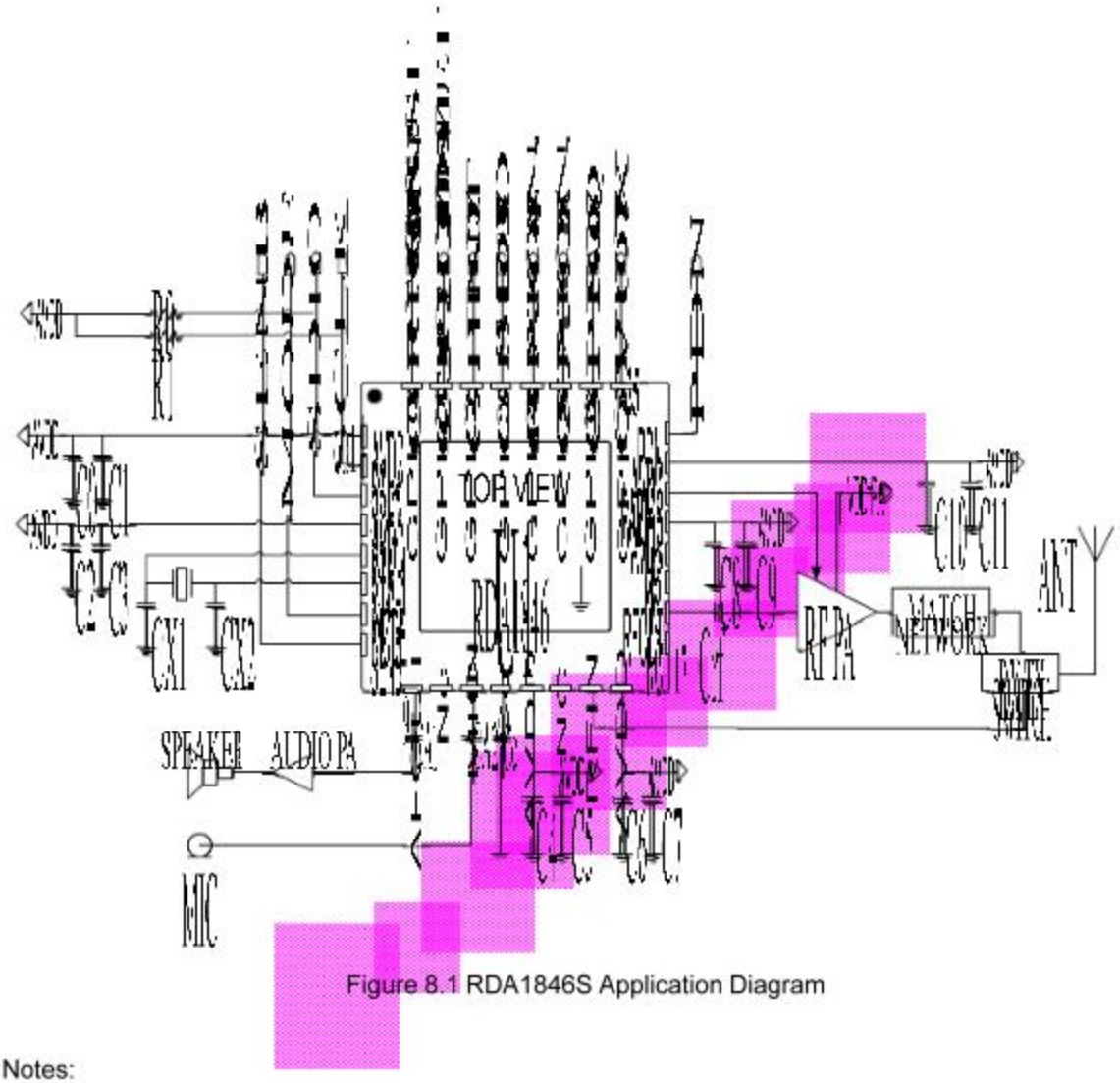


Figure 8.1 RDA1846S Application Diagram

Notes:

1 U1: RDA1846S Chip;

2 AVDD: Power Supply for RDA1846S (3.3~4.8V);

3 AVDD_PA: Power Supply for RF PA, its voltage depends on the actual PA design;

4 C0~C11: AVDD decouple capacitance (1nF and 100nF in pairs), as close to AVDD pin as possible;

5 CA1~CA2: Audio AC couple capacitance (~47uF);

6 Cc: Compensation capacitance connected between pin Cc and GND (~47uF);

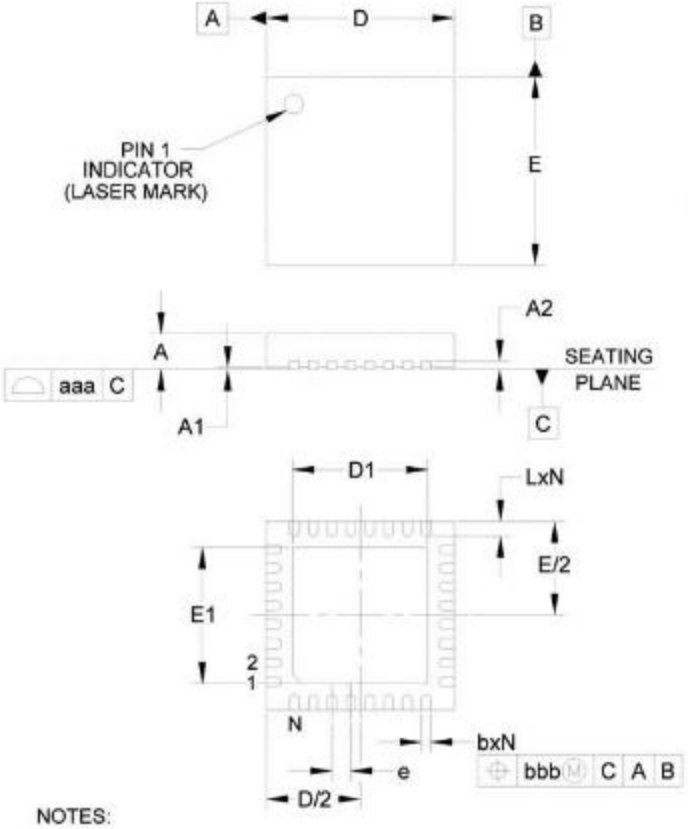
7 Crf: RF AC couple capacitance (~150pF);

8 CX1~CX2: XTAL oscillator load capacitance. Its value depends on the chosen XTAL *(if using external TCXO, clk should be sent into pin XTAL1 with Vpp about 1.5V, and pin XTAL2 should be connected to GND)* ;

9 R0~R1(optional): resistors for serial interface wire SDIO and SCLK (~10k Ω);

10 Pins NC(10,14,17,19,20) should be floating;

9. Package Outline



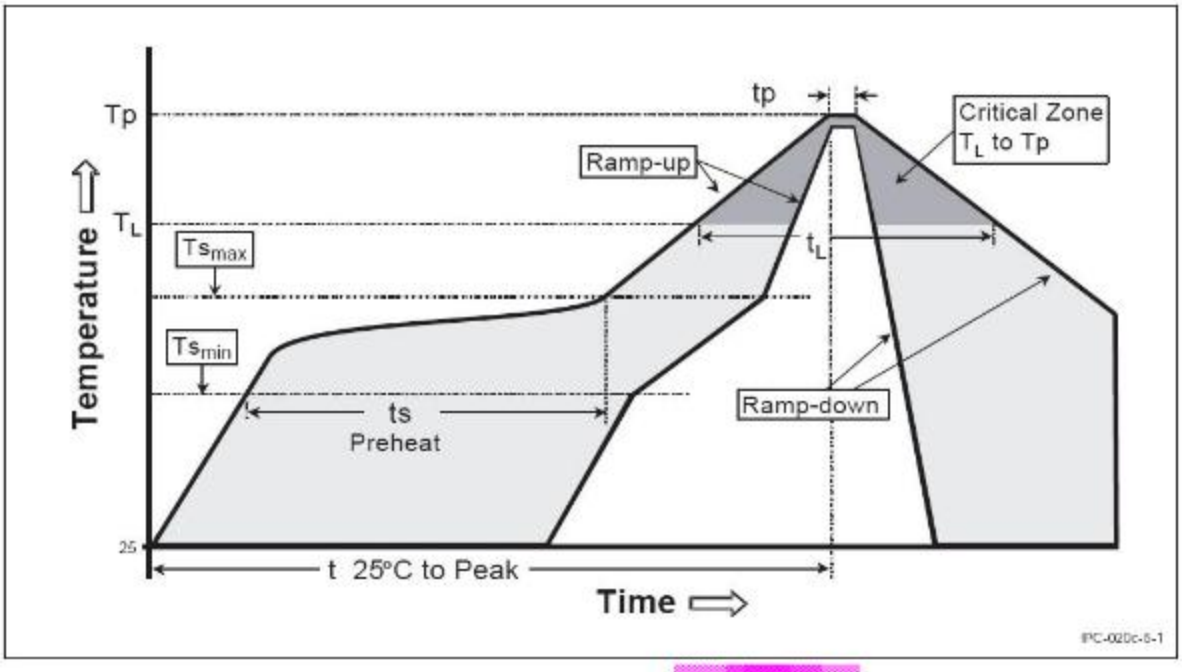
DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.130	.136	.140	3.30	3.45	3.55
E	.193	.197	.201	4.90	5.00	5.10
E1	.130	.136	.140	3.30	3.45	3.55
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

32-Pin 5x5 Quad Flat No-Lead (QFN)

10. Solder Mounting Condition



Classification Reflow Profile

Table 10-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table 10-2 SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table 10-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

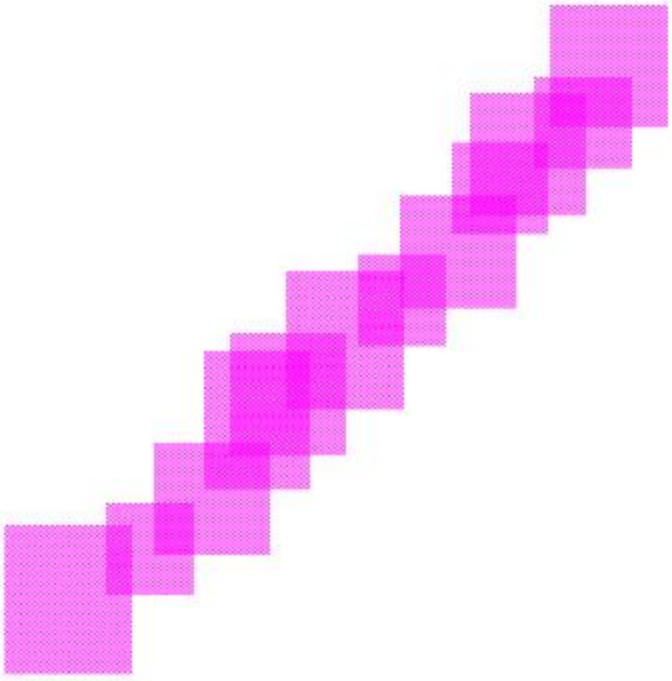
Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.



11. Change List

REV	DATE	AUTHER	CHANGE DESCRIPTION
V0.1	2011-8-23	Liu Ge	Original draft.

12. Contact Information

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