

General purpose operational amplifier

μ A741/ μ A741C/SA741C

DESCRIPTION

The μ A741 is a high performance operational amplifier with high open-loop gain, internal compensation, high common mode range and exceptional temperature stability. The μ A741 is short-circuit-protected and allows for nulling of offset voltage.

FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range

PIN CONFIGURATION

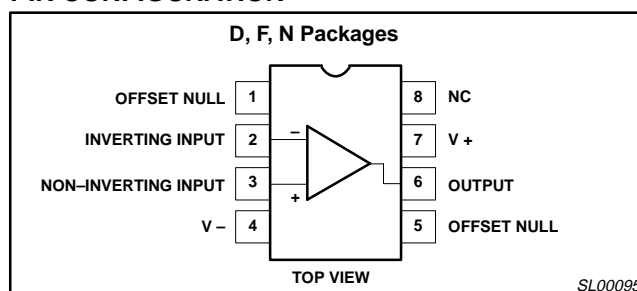


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	μ A741N	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	μ A741CN	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA741CN	SOT97-1
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	μ A741F	0580A
8-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	μ A741CF	0580A
8-Pin Small Outline (SO) Package	0 to +70°C	μ A741CD	SOT96-1

ABSOLUTE MAXIMUM RATINGS

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SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage μ A741C μ A741	± 18 ± 22	V V
P_D	Internal power dissipation D package N package F package	780 1170 800	mW mW mW
V_{IN}	Differential input voltage	± 30	V
V_{IN}	Input voltage ¹	± 15	V
I_{SC}	Output short-circuit duration	Continuous	
T_A	Operating temperature range μ A741C SA741C μ A741	0 to +70 -40 to +85 -55 to +125	°C °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

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DC ELECTRICAL CHARACTERISTICS

 $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μ A741			μ A741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10\text{k}\Omega$ $R_S = 10\text{k}\Omega$, over temp.		1.0 1.0 10	5.0 6.0		2.0 10	6.0 7.5	mV mV $\mu\text{V}/^\circ\text{C}$
I_{OS}	Offset current	Over temp. $T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$		20 7.0 20 200	200 200 500		20 200	200 300	nA nA nA $\text{pA}/^\circ\text{C}$
$\Delta I_{OS}/\Delta T$									
I_{BIAS}	Input bias current	Over temp. $T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$		80 30 300 1	500 500 1500		80 1	500 800	nA nA nA $\text{nA}/^\circ\text{C}$
$\Delta I_B/\Delta T$									
V_{OUT}	Output voltage swing	$R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$, over temp.	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V V
A_{VOL}	Large-signal voltage gain	$R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$ $R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$, over temp.	50 25	200		20 15	200		V/mV V/mV
	Offset voltage adjustment range			± 30			± 30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$ $R_S \leq 10\text{k}\Omega$, over temp.					10	150	$\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$
CMRR	Common-mode rejection ratio	Over temp.	70	90		70	90		dB dB
I_{CC}	Supply current	$T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$		1.4 1.5 2.0	2.8 2.5 3.3		1.4	2.8	mA mA mA
V_{IN}	Input voltage range	(μ A741, over temp.)	± 12	± 13		± 12	± 13		V
R_{IN}	Input resistance		0.3	2.0		0.3	2.0		M Ω
P_D	Power consumption	$T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$		50 45 45	85 75 100		50	85	mW mW mW
R_{OUT}	Output resistance			75			75		Ω
I_{SC}	Output short-circuit current		10	25	60	10	25	60	mA

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SYMBOL	PARAMETER	TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10\text{k}\Omega$		2.0	6.0	mV
$\Delta V_{OS}/\Delta T$		$R_S = 10\text{k}\Omega$, over temp.		10	7.5	mV/ $^\circ\text{C}$
I_{OS}	Offset current	Over temp.		20	200	nA
$\Delta I_{OS}/\Delta T$				200	500	pA/ $^\circ\text{C}$
I_{BIAS}	Input bias current	Over temp.		80	500	nA
$\Delta I_B/\Delta T$				1	1500	nA/ $^\circ\text{C}$
V_{OUT}	Output voltage swing	$R_L = 10\text{k}\Omega$	± 12	± 14		V
		$R_L = 2\text{k}\Omega$, over temp.	± 10	± 13		V
A_{VOL}	Large-signal voltage gain	$R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	20	200		V/mV
		$R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$, over temp.	15			V/mV
	Offset voltage adjustment range			± 30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$		10	150	$\mu\text{V/V}$
CMRR	Common mode rejection ratio		70	90		dB
V_{IN}	Input voltage range	Over temp.	± 12	± 13		V
R_{IN}	Input resistance		0.3	2.0		M Ω
P_d	Power consumption			50	85	mW
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μ A741, μ A741C			UNIT
			Min	Typ	Max	
R_{IN}	Parallel input resistance	Open-loop, $f = 20\text{Hz}$	0.3			M Ω
C_{IN}	Parallel input capacitance	Open-loop, $f = 20\text{Hz}$		1.4		pF
	Unity gain crossover frequency	Open-loop		1.0		MHz
t_R	Transient response unity gain	$V_{IN} = 20\text{mV}$, $R_L = 2\text{k}\Omega$, $C_L \leq 100\text{pF}$				
	Rise time			0.3		μs
	Overshoot			5.0		%
SR	Slew rate	$C \leq 100\text{pF}$, $R_L \geq 2\text{k}\Omega$, $V_{IN} = \pm 10\text{V}$		0.5		V/ μs

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The diagram shows a fully differential operational amplifier circuit. It features two input terminals: 'NON-INVERTING INPUT' and 'INVERTING INPUT'. The non-inverting input is connected to a differential pair of transistors (Q1, Q2) and a tail resistor R1 (1KΩ). The inverting input is connected to a differential pair (Q8, Q9) and a tail resistor R3 (50KΩ). The output of the non-inverting input stage is connected to the inverting input of the second stage (Q12, Q13). The output of the inverting input stage is connected to the non-inverting input of the second stage (Q16, Q17). The second stage also has a tail resistor R4 (5kΩ). The output of the second stage is connected to the output terminal 'OUTPUT' through a resistor R9 (25Ω). The output is also connected to a feedback network consisting of a capacitor (30pF) and a resistor R7 (4.5Ω) in parallel, followed by a resistor R8 (7.5KΩ) in series. The output is also connected to a resistor R10 (50Ω) to the negative supply V-. The circuit includes an 'OFFSET NULL' input, which is connected to a differential pair of transistors (Q5, Q6) and a tail resistor R2 (1KΩ). The offset null input is also connected to a differential pair of transistors (Q10, Q11) and a tail resistor R4 (5kΩ). The circuit is powered by a positive supply V+ and a negative supply V-.

Figure 2. Equivalent Schematic

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TYPICAL PERFORMANCE CHARACTERISTICS

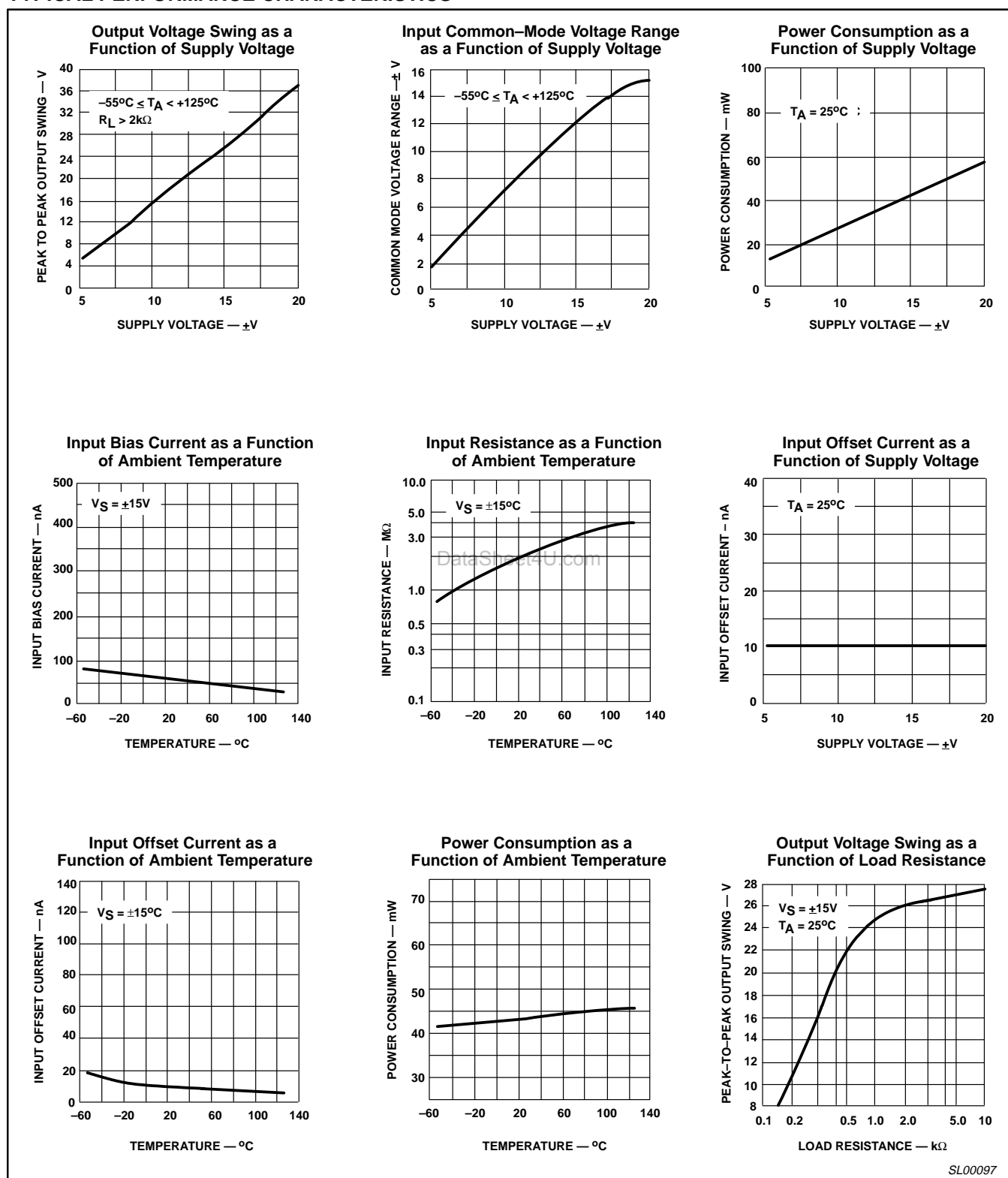


Figure 3. Typical Performance Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

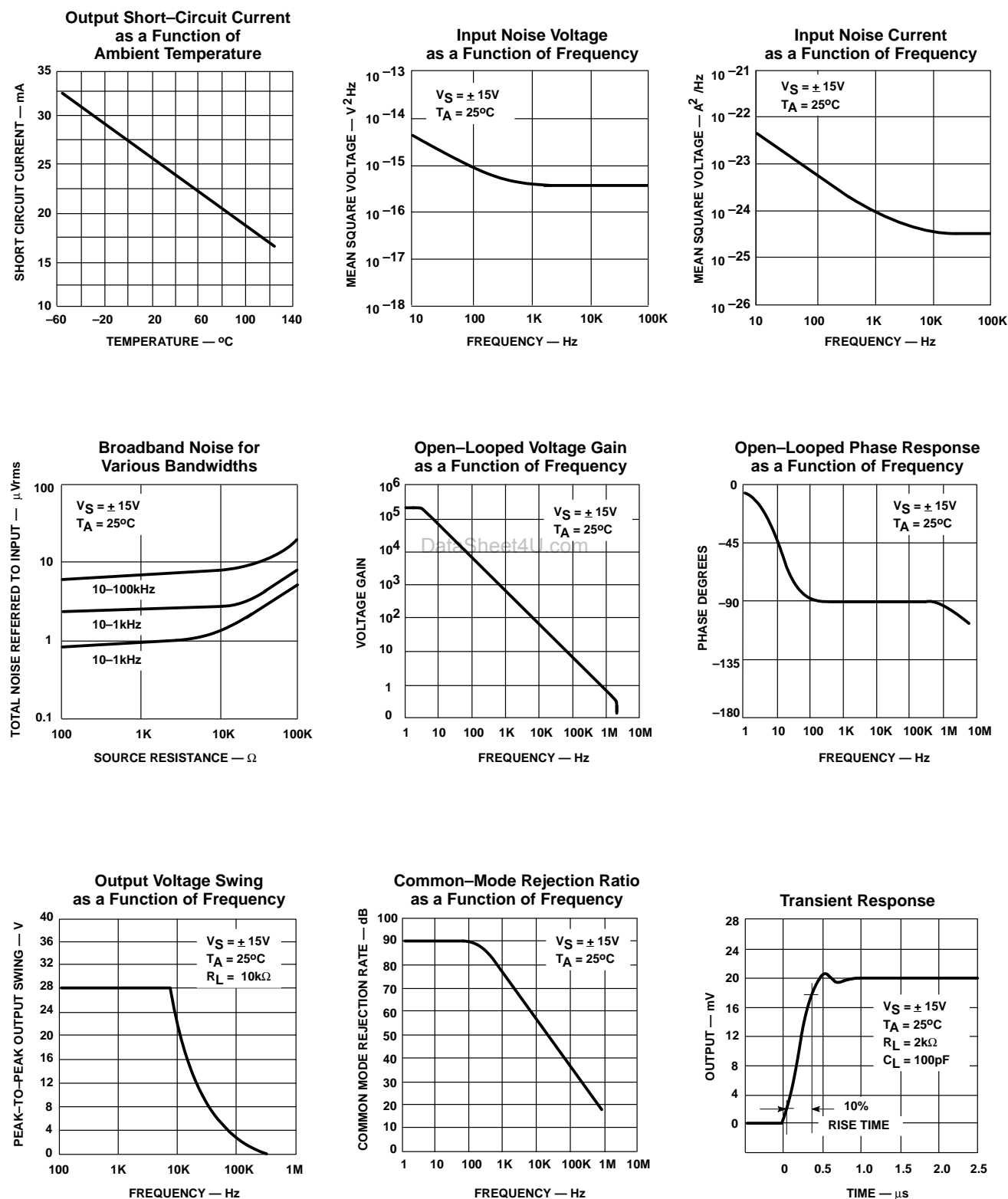


Figure 4. Typical Performance Characteristics (cont.)

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

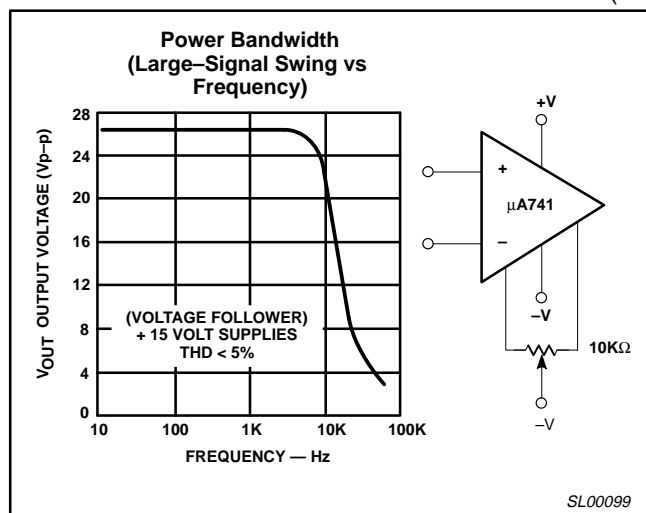


Figure 5. Typical Performance Characteristics (cont.)