



## N-Channel Enhancement-Mode Vertical DMOS Power FETs

T-39-05

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package				
			TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP
40V	2Ω	3.0A	VN0204N2	—	VN0204N5	VN0240N6	VN0204N7
60V	2Ω	3.0A	VN0206N2	VN0206N3	VN0206N5	VN0206N6	VN0206N7
100V	2Ω	3.0A	VN0210N2	VN0210N3	VN0210N5	—	—

### Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C<sub>iss</sub> and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

### Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

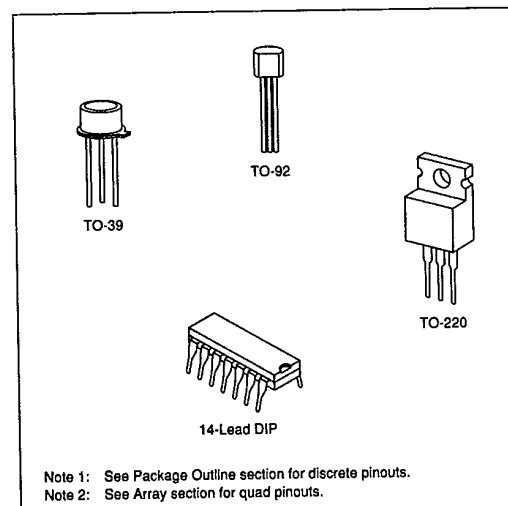
### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\*Distance of 1.6 mm from case for 10 seconds.

### Package Options

(Notes 1 and 2)



## Thermal Characteristics

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Package	$I_D$ (continuous)*	$I_D$ (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{JA}$ $^\circ\text{C/W}$	$\theta_{JB}$ $^\circ\text{C/W}$	$I_{DR}$	$I_{DRM}$ *
TO-39	1.5A	4A	4W	25	125	2A	4A
TO-92	0.8A	4A	1W	125	170	0.8A	4A
TO-220	3.0A	4A	28W	4.8	70	3A	4A
Plastic Dip	Refer to Arrays and Special Functions section.						
Ceramic Dip							

\* $I_D$  (continuous) is limited by max rated  $T_J$ .Electrical Characteristics (@  $25^\circ\text{C}$  unless otherwise specified)

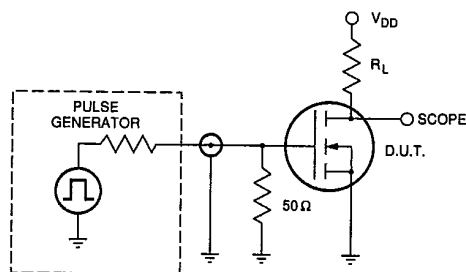
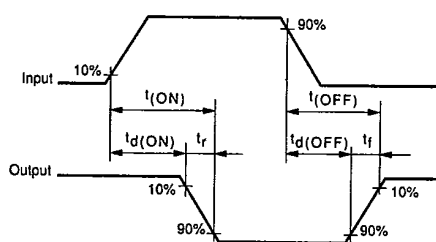
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	VN0204	40		V	$V_{GS} = 0, I_D = 2.5\text{mA}$
		VN0206	60			
		VN0210	100			
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{GS} = V_{DS}, I_D = 2.5\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.8	-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 2.5\text{mA}$
$I_{GSS}$	Gate Body Leakage			100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
$I_{DSS}$	Zero Gate Voltage Drain Current			25	$\mu\text{A}$	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				1	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	1.2	1.6		A	$V_{GS} = 5\text{V}, V_{DS} = 25\text{V}$
		3.0	4.0			$V_{GS} = 10\text{V}, V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		1.6	2.5	$\Omega$	$V_{GS} = 5\text{V}, I_D = 1\text{A}$
			1.5	2		$V_{GS} = 10\text{V}, I_D = 2\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.5	0.75	%/ $^\circ\text{C}$	$V_{GS} = 10\text{V}, I_D = 2\text{A}$
$G_{FS}$	Forward Transconductance	0.4	0.65		$\text{S}$	$V_{DS} = 25\text{V}, I_D = 2\text{A}$
$C_{ISS}$	Input Capacitance		85	150	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance		50	85		
$C_{RSS}$	Reverse Transfer Capacitance		12	35		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25\text{V}$ $I_D = 0.5\text{A}$ $R_S = 50\Omega$
$t_r$	Rise Time			10		
$t_{d(OFF)}$	Turn-OFF Delay Time			25		
$t_f$	Fall Time			13		
$V_{SD}$	Diode Forward Voltage Drop		1.2	1.8	V	$V_{GS} = 0, I_{SD} = 1.5\text{A}$
$t_{rr}$	Reverse Recovery Time		330		ns	$V_{GS} = 0, I_{SD} = 1\text{A}$

Note 1: All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

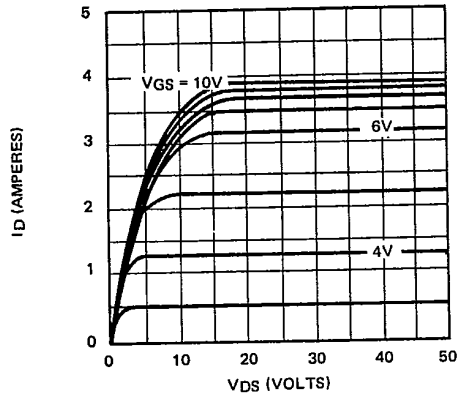
## Switching Waveforms and Test Circuit



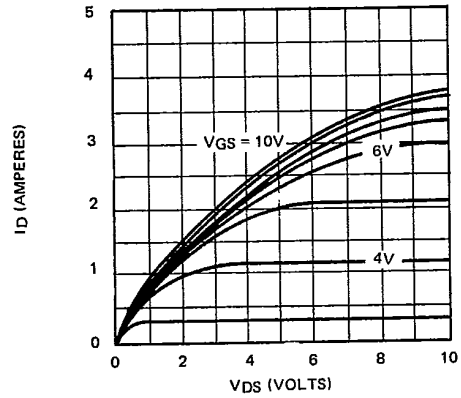
# Typical Performance Curves

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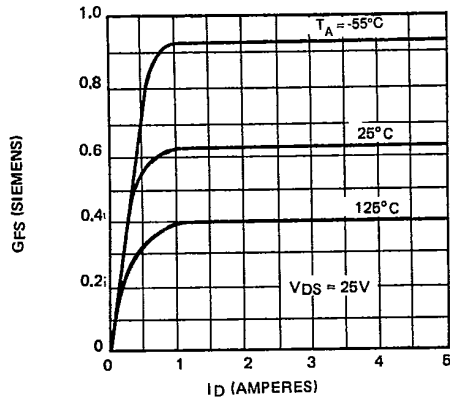
Output Characteristics



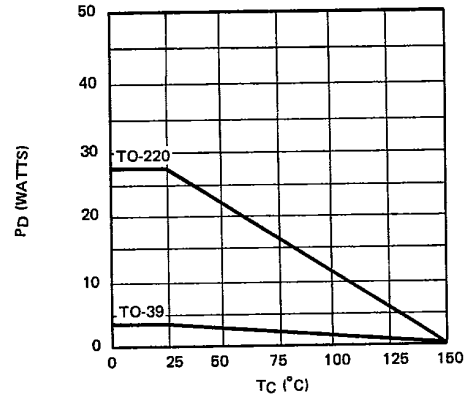
Saturation Characteristics



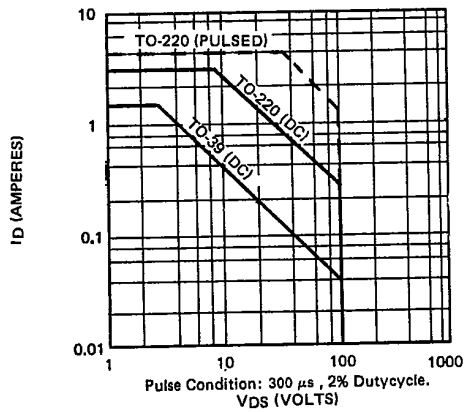
Transconductance Vs. Drain Current



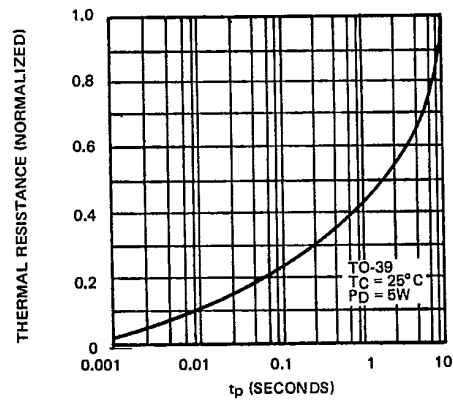
Power Dissipation Vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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