

**Version : 3.0****TECHNICAL SPECIFICATION****MODEL NO : PW056XU2**

The content of this information is subject to be changed without notice.

Please contact PVI or its agent for further information.

☐ Customer's Confirmation

Customer \_\_\_\_\_

Date \_\_\_\_\_

By \_\_\_\_\_

☐ PVI's Confirmation

Confirmed By \_\_\_\_\_



Prepared By \_\_\_\_\_



## ***Revision History***

<b>Rev.</b>	<b>Issued Date</b>	<b>Revised Contents</b>
1.0	May 23, 2007	New
2.0	Nov.15.2007	Page 4:Modify the reference, refer to Note 10-1 Page 19>Delete the item b) of 11-1 Page 24:Modify the Packing diagram
3.0	March.24.2008	Add Page 21 11.Handling Cautions 11-1 item d)

# TECHNICAL SPECIFICATION

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## 1. Application

This technical specification applies to 5.6" color TFT-LCD module, PW056XU2.

The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system.

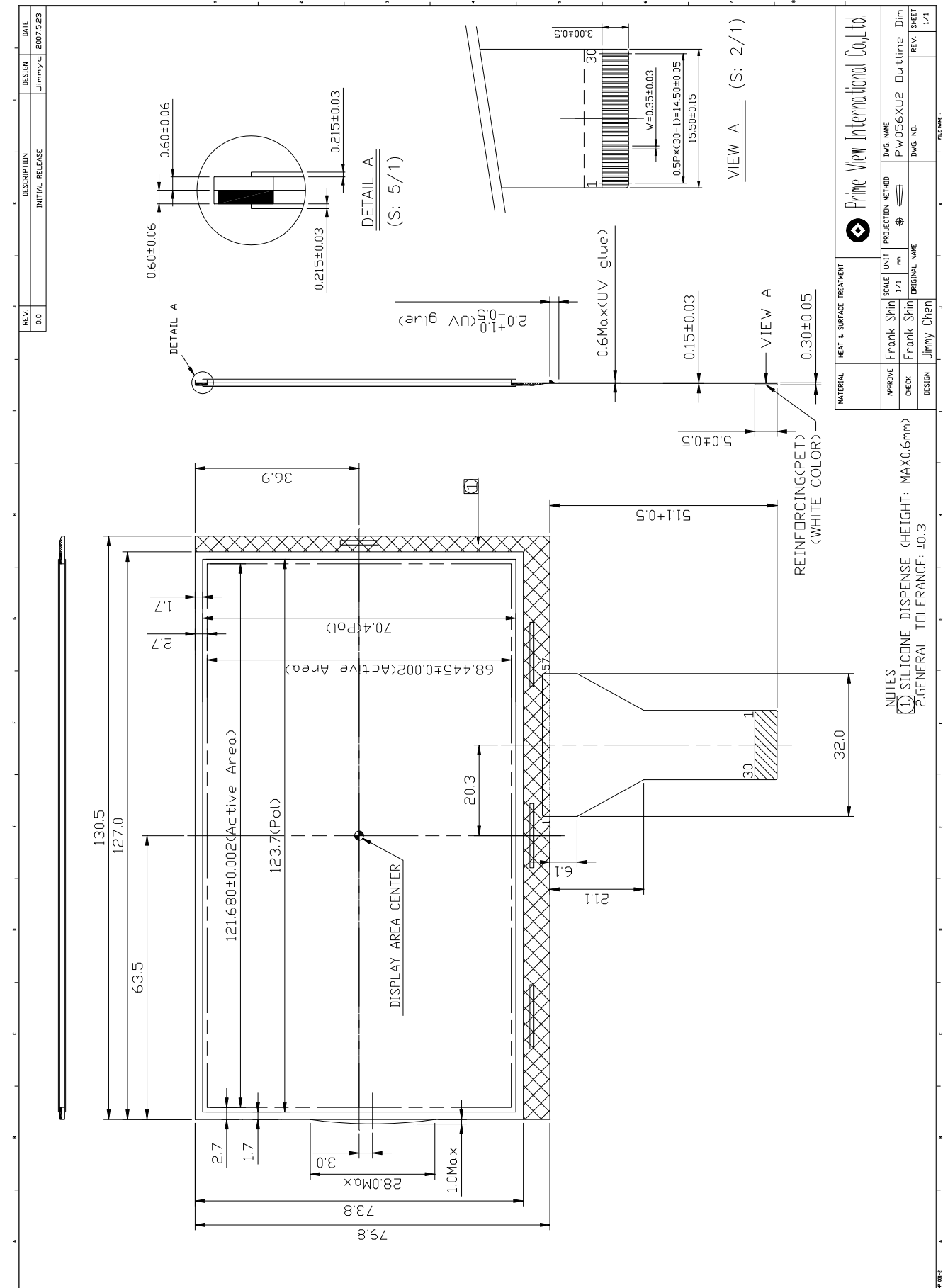
## 2. Features

- . Pixel in stripe configuration
- . Compatible with NTSC and PAL system
- . Slim and compact
- . Up / Down and Left / Right Image Reversal
- . Support full , center , wide mode with PVI-1004D  
(If customer use PVI-1004D , this panel doesn't support zoom mode)

## 3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	5.6 (16 : 9 diagonal)	Inch
Display Format	480×(R,G,B)×234	Dot
Active Area	121.680 (H)×68.445 (V)	mm
Pixel Pitch	0.2535 (H)×0.2925 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	130.5 (W)× 79.8(H)× 1.63(D) (typ.)	mm
Weight	34±4	g
Surface Treatment	Anti-Glare	
Display mode	Normally white	
Gray scale inversion direction	6 o'clock (ref to Note 10-1)	

# 4. Mechanical Drawing of TFT-LCD Module



## 5. Input / Output Terminals

LCD Module Connector

FPC Down Connect , 30 Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V <sub>CC</sub>	I	Supply voltage of logic control circuit for gate driver	Note 5-2
3	NC	-	No connection	
4	V <sub>EE</sub>	I	Negative power for gate driver	Note 5-3
5	NC	-	No connection	
6	V <sub>GH</sub>	I	Positive power for gate driver	Note 5-3
7	NC	-	No connection	
8	STVD	I/O	Vertical start pulse	Note 5-5
9	STVU	I/O	Vertical start pulse	
10	CKV	I	Shift clock for gate driver	
11	U/D	I	Up / Down Control for gate driver	Note 5-5
12	OE3	I	Output enable for gate driver	
13	OE2	I	Output enable for gate driver	
14	OE1	I	Output enable for gate driver	
15	V <sub>COM</sub>	I	Common electrode voltage	Note 5-1
16	STHL	I/O	Start pulse for source driver	Note 5-5
17	V <sub>SS2</sub>	-	Ground for analog circuit	
18	V <sub>R</sub>	I	Video Input R	
19	V <sub>G</sub>	I	Video Input G	
20	V <sub>B</sub>	I	Video Input B	
21	V <sub>SS1</sub>	-	Ground for digital circuit	
22	V <sub>DD2</sub>	I	Supply power for analog circuit	Note 5-4
23	CPH1	I	Sampling and shift clock for source driver	Note 5-6
24	CPH2	I	Sampling and shift clock for source driver	
25	CPH3	I	Sampling and shift clock for source driver	
26	V <sub>DD1</sub>	I	Supply power for digital circuit	Note 5-2
27	R/L	I	Left / Right Control for source driver	Note 5-5
28	NC	I	No Connection	
29	OE <sub>H</sub>	I	Output enable for source driver	
30	STHR	I/O	Start pulse for source driver	Note 5-5

Note 5-1 :  $V_{COM (TYP.)} = +5V$

Phase of the video signal input and  $V_{COM}$

The relation between these values could refer to 8-1 Operating condition.

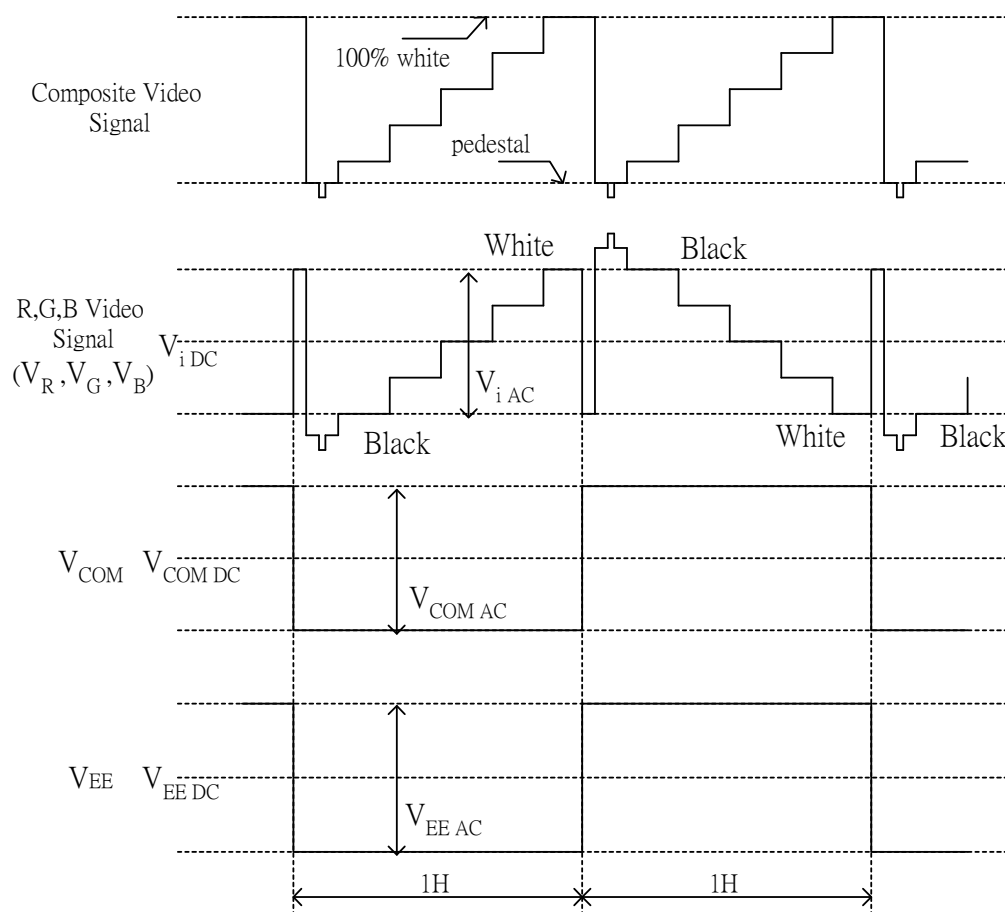


Fig.1

Liquid crystal transmission of the video signal input,  $V_{COM}$  and timing

	$V_{COM}$	
	H Level	L Level
Video Signal Input Maximum	Black	White
Video Signal Input Minimum	White	Black

White : maximum transmission / Black : minimum transmission

Note 5-2 :  $V_{CC}, V_{DD1 (TYP.)} = +3.3V$

Note 5-3 :  $V_{EE (TYP.)} = -12V$  ;  $V_{GH (TYP.)} = +17V$

Note 5-4 :  $V_{DD2 (TYP.)} = +5V$

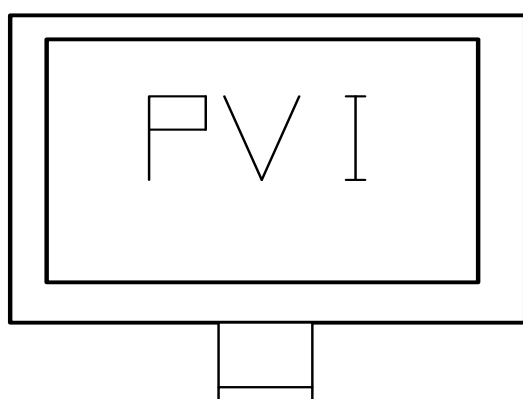
Note 5 – 5 : STHL, STHR and R/L mode

R/L	STHR	STHL	Remark
High( $V_{DD1}$ )	Input	Output	Left to Right
GND	Output	Input	Right to Left

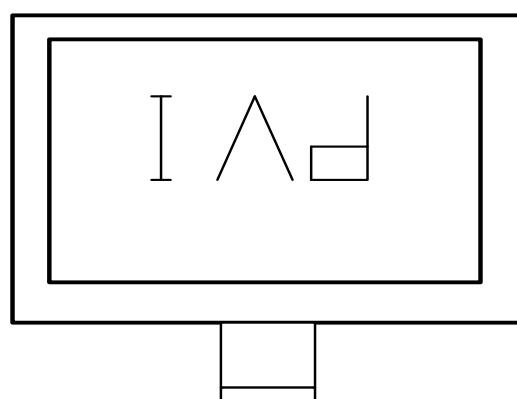
STVD, STVU and U/D mode

U/D	STVD	STVU	Remark
High( $V_{CC}$ )	Input	Output	Down to Up
GND	Output	Input	Up to Down

U/D(PIN 11)=Low R/L(PIN 27)=High

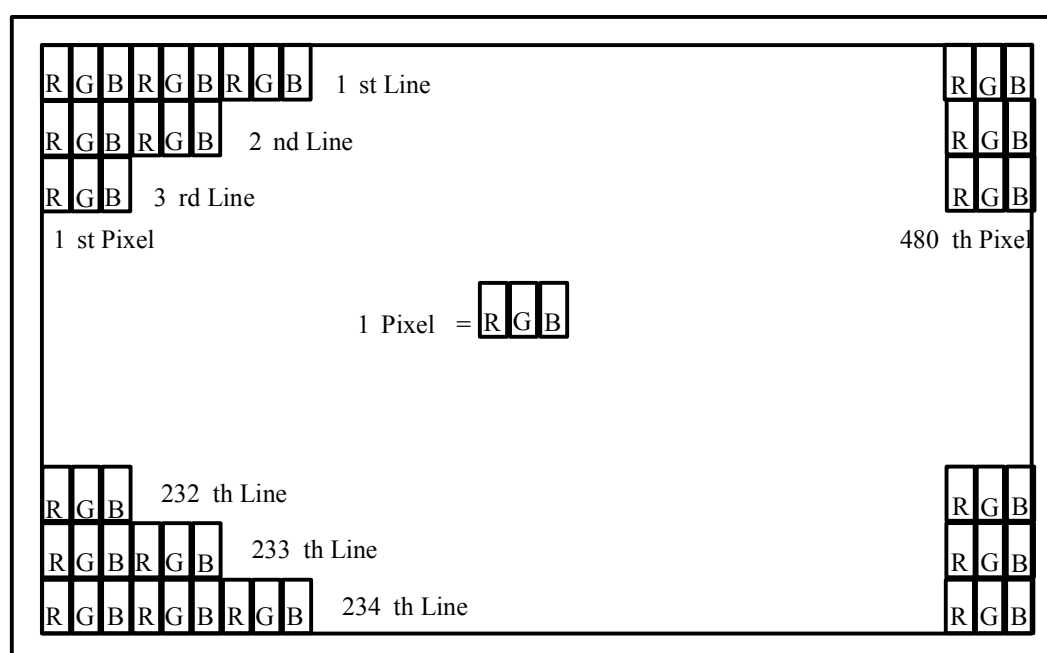


U/D(PIN 11)=High R/L(PIN 27)=Low



Note 5-6 : The CPH1 reference Fig.8-1 Sampling clock timing  
CPH2 and CPH3 connect GND.

## 6. Pixel Arrangement





## 7. Absolute Maximum Ratings

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

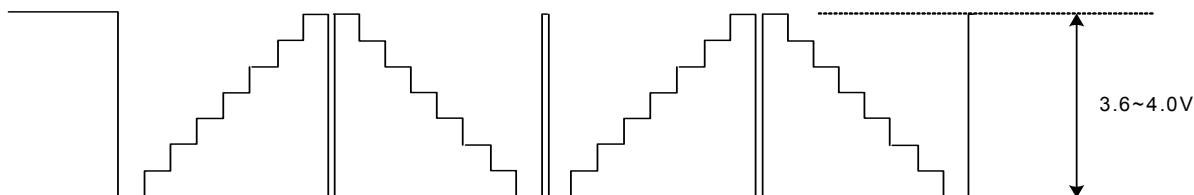
Parameter	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage for Source Driver	$V_{DD2}$	-0.3	+5.8	V	
	$V_{DD1}$	-0.3	+7.0	V	
Supply Voltage for Gate Driver	$V_{CC}$	-0.3	+7.0	V	
	$V_{GH}-V_{EE}$	-0.3	+45.0	V	
	H Level $V_{GH}$	-0.3	+30.0	V	
	L Level $V_{EE}$	-17	+0.3	V	

## 8. Electrical Characteristics

### 8-1) Recommended Driving condition for TFT-LCD panel

Parameter	Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage for Source Driver	Analog $V_{DD2}$	+4.5	+5.0	+5.5	V	
	Logic $V_{DD1}$	+3.0 +4.5	+3.3 +5.0	+3.6 +5.5	V V	Depend on T/C signal voltage
Supply Voltage for Gate Driver	$V_{GH}$	+15	+17	+19	V	
	$V_{EE\ DC}$	-13.0	-12	-10.5	V	DC Component of $V_{EE}$
	$V_{EE\ AC}$	-	+5.0	-	$V_{P-P}$	AC Component of $V_{EE}$
	Logic $V_{CC}$	+3.0 +4.5	+3.3 +5.0	+3.6 +5.5	V V	Depend on T/C signal voltage
Analog Signal input Level ( $V_R, V_G, V_B$ )	$V_{iAC}$	-	+3.6	+4.0	V	Note 8-1
	$V_{iDC}$	-	2.5	-	V	
Digital input voltage	H level $V_{IH}$	0.7 $V_{DD1}$	-	$V_{DD1}$	V	
	L level $V_{IL}$	-0.3	-	0.3 $V_{DD1}$	V	
Digital output voltage	H level $V_{OH}$	0.7 $V_{DD1}$	-	$V_{DD1}$	V	
	L level $V_{OL}$	-0.3	-	0.3 $V_{DD1}$	V	
$V_{COM}$	$V_{COM\ AC}$	-	5.0	-	$V_{P-P}$	AC Component of $V_{COM}$
	$V_{COM\ DC}$	-	1.9	-	V	DC Component of $V_{COM}$ . Note 8-2

Note 8-1: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.



Note 8-2 : PVI strongly suggests that the  $V_{COM\ DC}$  level shall be adjustable , and the adjustable level range is  $1.9V \pm 1V$  , every module's  $V_{COM\ DC}$  level shall be carefully adjusted to show a best image performance.

## 8-2) Power Consumption

Ta= 25 °C

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I <sub>GH</sub>	V <sub>GH</sub> = +17V	0.068	0.204	mA	
Supply current for Gate Driver (Low level)	I <sub>EE</sub>	V <sub>EE</sub> = -12V	0.134	0.402	mA	V <sub>EE</sub> center voltage
Supply current for Source Driver(Digital)	I <sub>DD1</sub>	V <sub>DD1</sub> = +3.3V	1.8	3.6	mA	
Supply current for Source Driver(Analog)	I <sub>DD2</sub>	V <sub>DD2</sub> = +5V	10.5	21	mA	
Supply current for Gate Driver (Digital)	I <sub>CC</sub>	V <sub>CC</sub> = +3.3V	0.004	0.012	mA	
LCD Panel Power Consumption	-	-	61.22	125.21	mW	Note 8-3

Note 8-3 : The power consumption for back light is not included.

## 8-3) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Rising time	t <sub>r</sub>	-	-	10	ns	
Falling time	t <sub>f</sub>	-	-	10	ns	
High and low level pulse width	t <sub>CPH</sub>	9.2	9.6	10.0	MHZ	CPH1~CPH3
CPH pulse duty	t <sub>CWH</sub>	30	50	70	%	CPH1~CPH3
STH setup time	t <sub>SUH</sub>	20	-	-	ns	STHR,STHL
STH hold time	t <sub>HDH</sub>	20	-	-	ns	STHR,STHL
STH pulse width	t <sub>STH</sub>	-	1	-	t <sub>CPH</sub>	STHR,STHL
STH period	t <sub>H</sub>	61.5	63.5	65.5	μs	STHR,STHL
OEH pulse width	t <sub>OEH</sub>	-	1.40	-	μs	OEH
Sample and hold disable time	t <sub>DIS1</sub>	-	7.43	-	μs	
OEV pulse width	t <sub>OEV</sub>	-	18	-	μs	OE1,2,3
CKV pulse width	t <sub>CKV</sub>	-	31.75	-	μs	CKV
Clean enable time	t <sub>DIS2</sub>	-	9.0	-	μs	
Horizontal display timing range	t <sub>DH</sub>	-	480	-	t <sub>CPH</sub>	
STV setup time	t <sub>SUV</sub>	400	-	-	ns	STVU,STVD
STV hold time	t <sub>HDV</sub>	400	-	-	ns	STVU,STVD
STV pulse width	t <sub>STV</sub>	-	-	1	t <sub>H</sub>	STVU,STVD
Horizontal lines per field	t <sub>V</sub>	256	262	268	t <sub>H</sub>	
Vertical display start	t <sub>SV</sub>	-	3	-	t <sub>H</sub>	
Vertical display timing range	t <sub>DV</sub>	-	234	-	t <sub>H</sub>	
VCOM rising time	t <sub>RCOM</sub>	-	-	5	μs	
VCOM falling time	t <sub>FCOM</sub>	-	-	5	μs	
VCOM delay time	t <sub>DCOM</sub>	-	-	3	μs	
RGB delay time	t <sub>DRGB</sub>	-	-	1	μs	

# 8-4) Signal Timing Waveforms

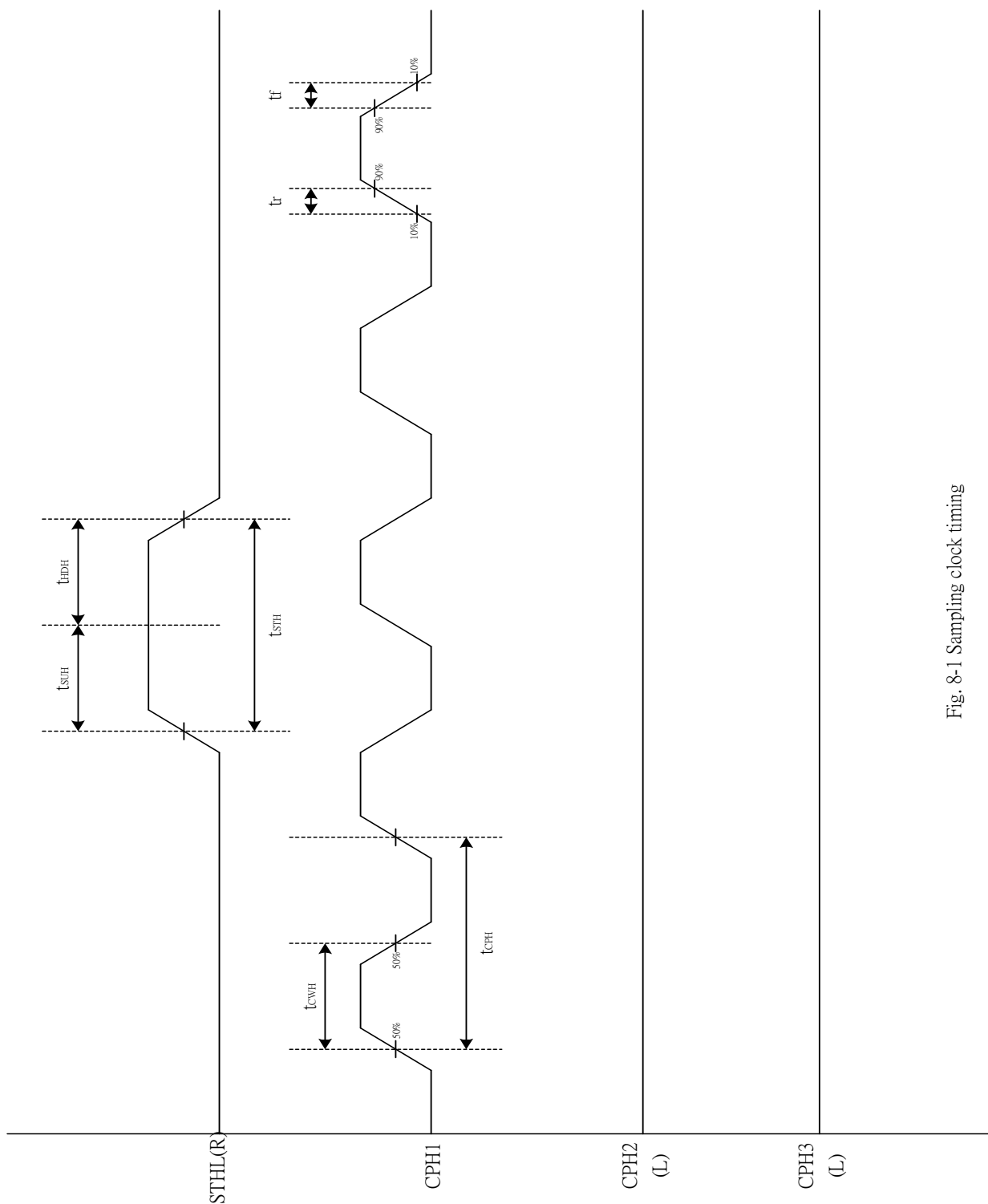


Fig. 8-1 Sampling clock timing

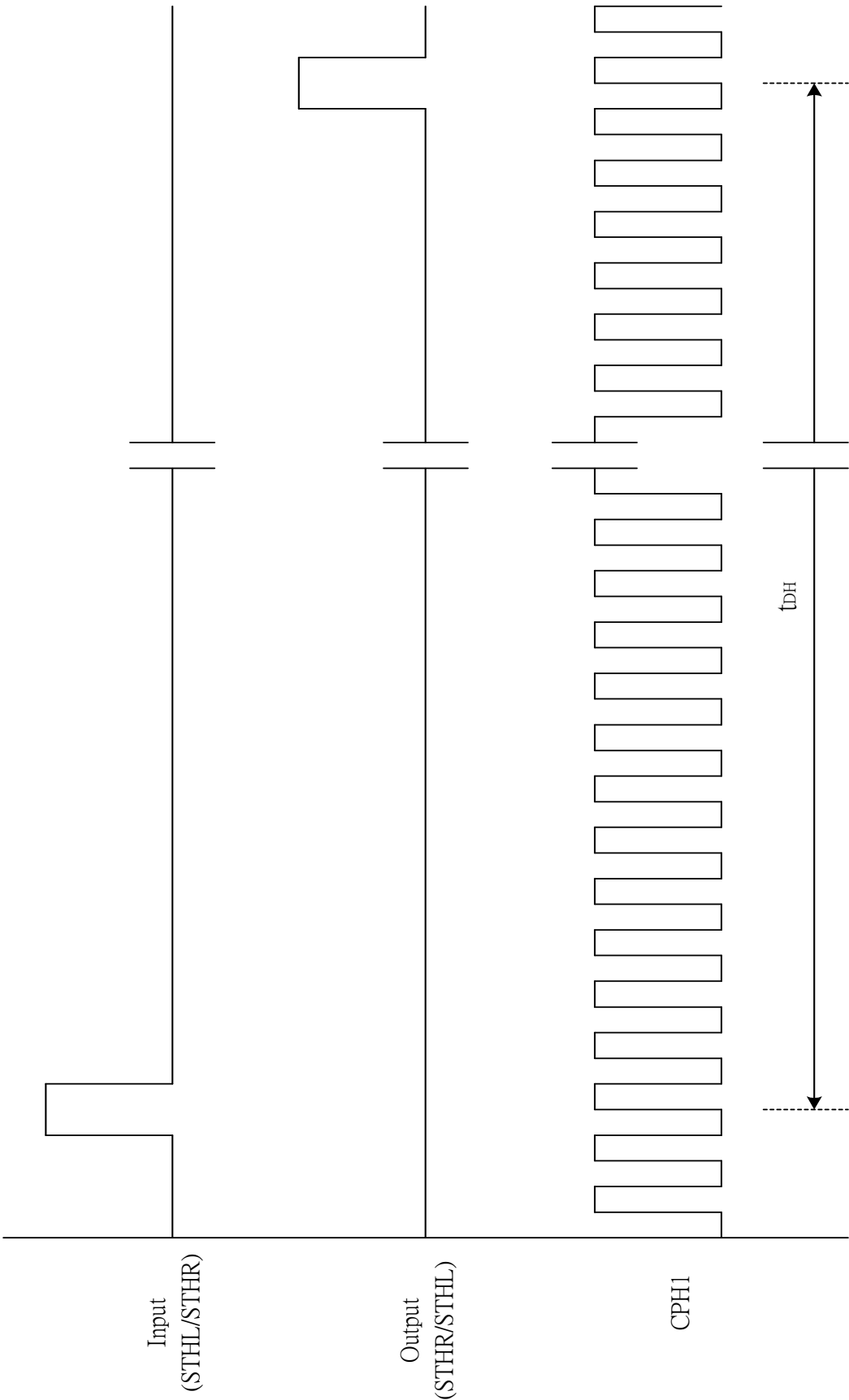


Fig. 8-2 Horizontal display timing range

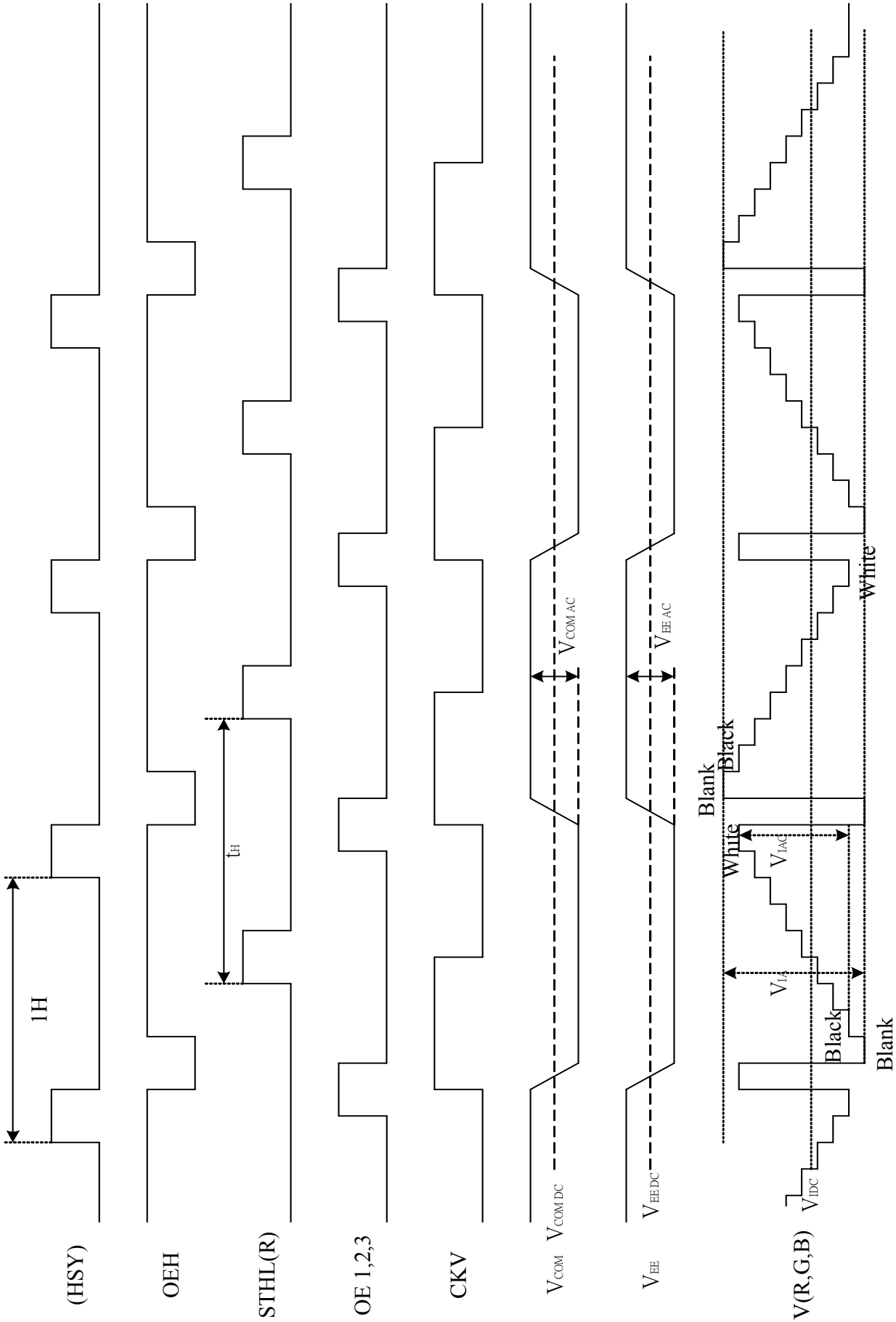
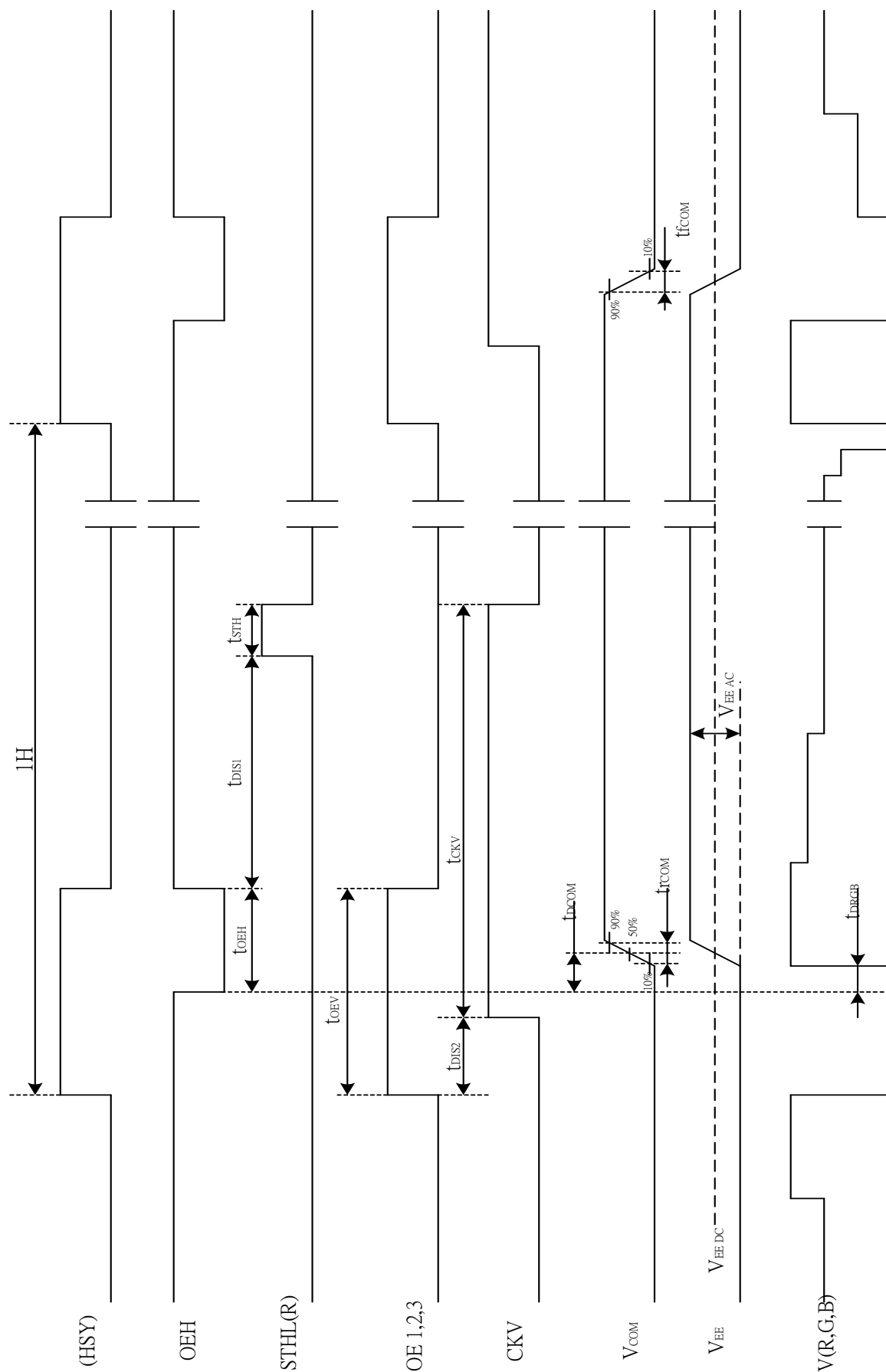


Fig. 8-3 (a) Horizontal timing



Note : The falling edge of OEVL should be synchronized with the falling edge of OEHL

Fig. 8-3 (b) Detail horizontal timing

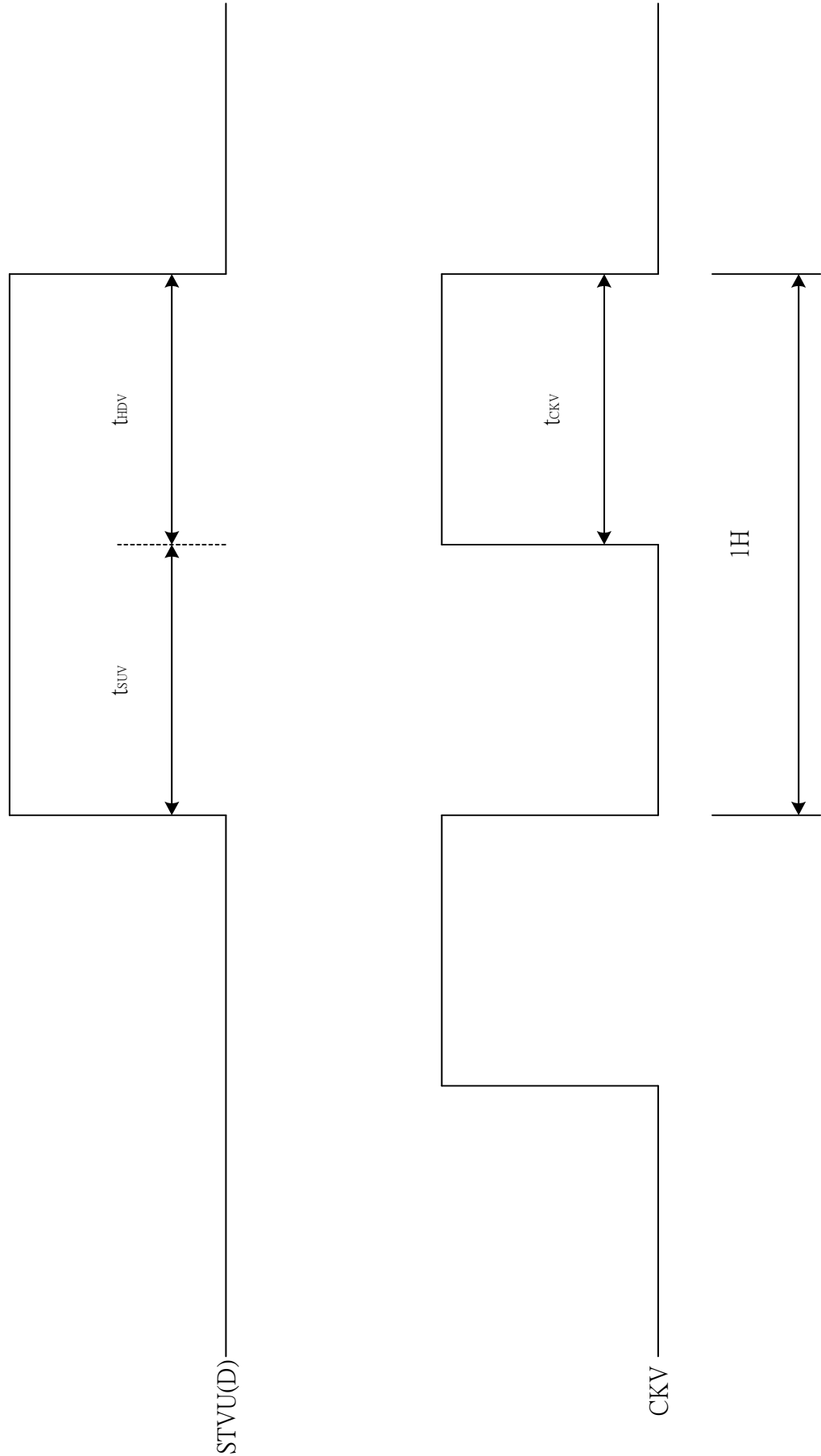


Fig. 8-4 Vertical shift clock timing

Vertical timing (From up to down)

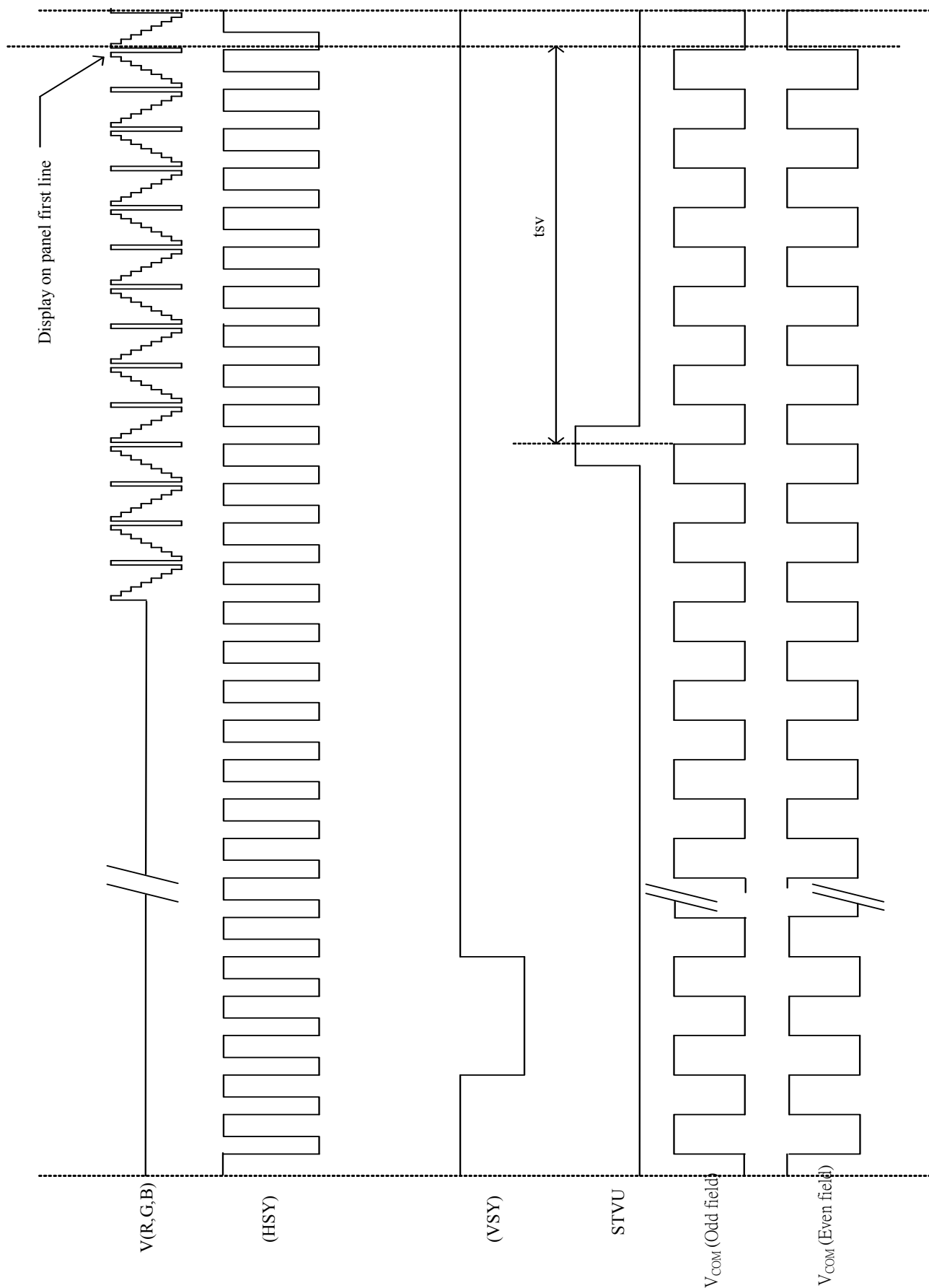


Fig. 8-5 (a) Vertical timing (From Up to Down)



Vertical timing (From down to up)

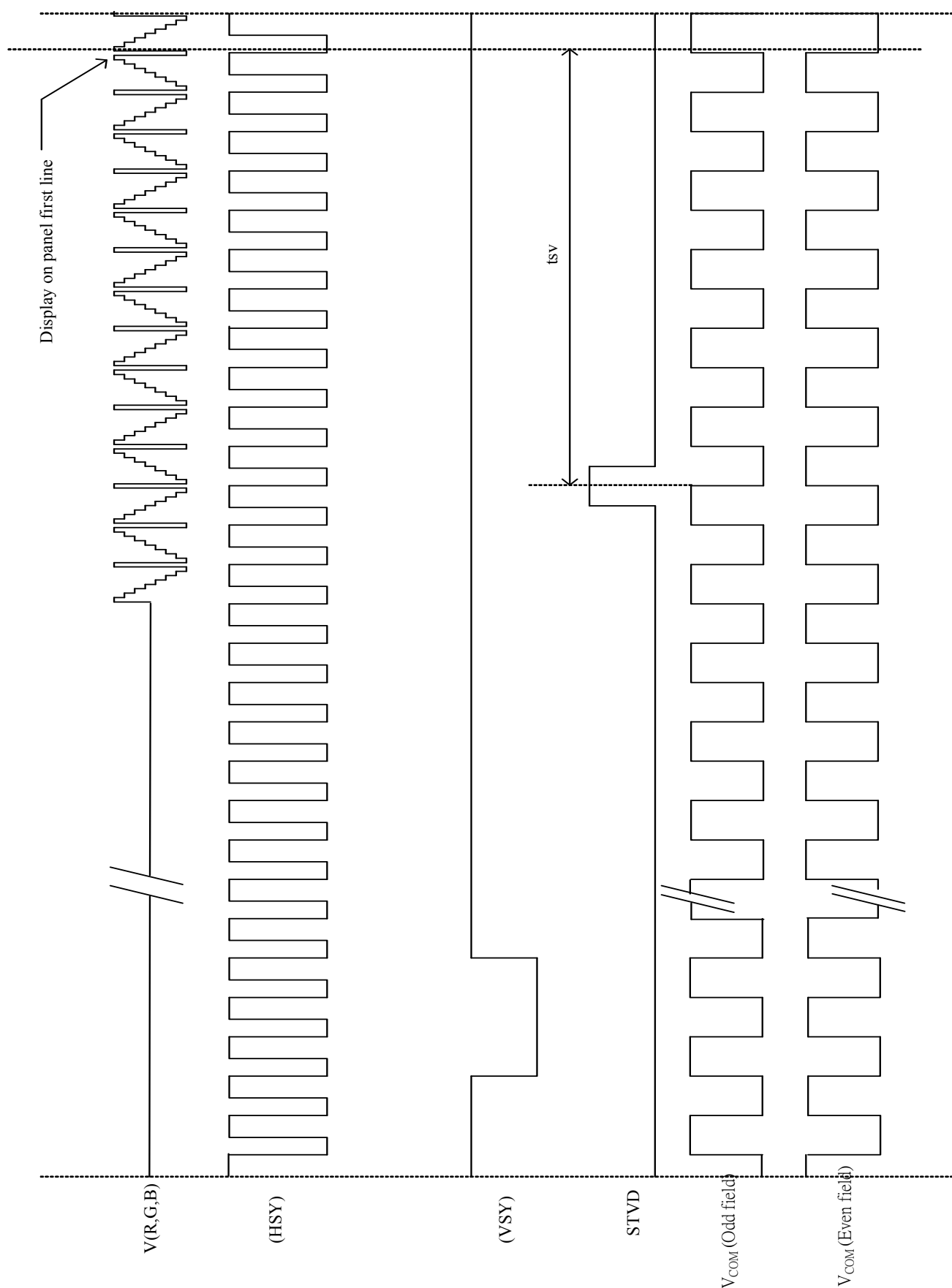
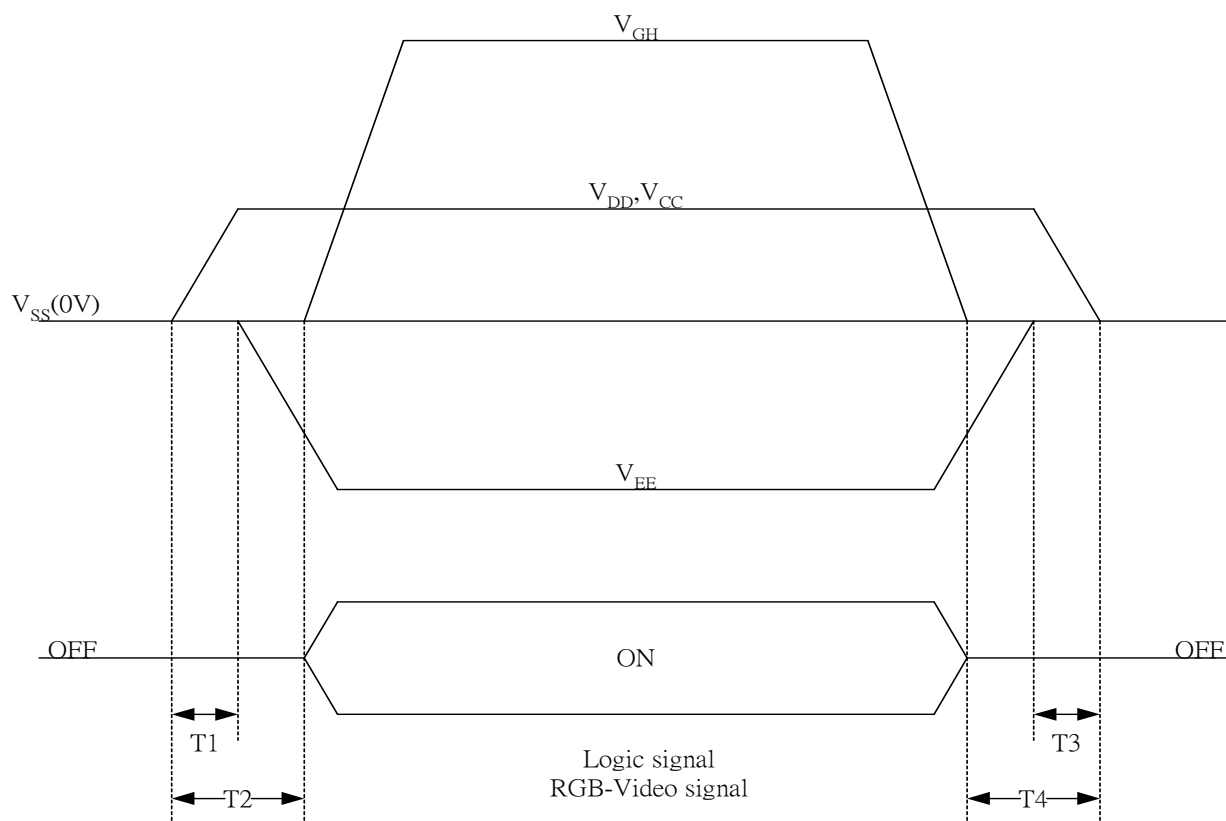


Fig. 8-5 (b) Vertical timing (From Down to Up)

## 9. Power on Sequence

The Power on Sequence only effect by  $V_{CC}$ ,  $V_{SS}$ ,  $V_{DD}$ ,  $V_{EE}$  and  $V_{GH}$ , the others do not care.



- 1)  $10\text{ms} \leq T1 < T2$
- 2)  $0\text{ms} < T3 \leq T4 \leq 10\text{ms}$

## 10. Optical Characteristics

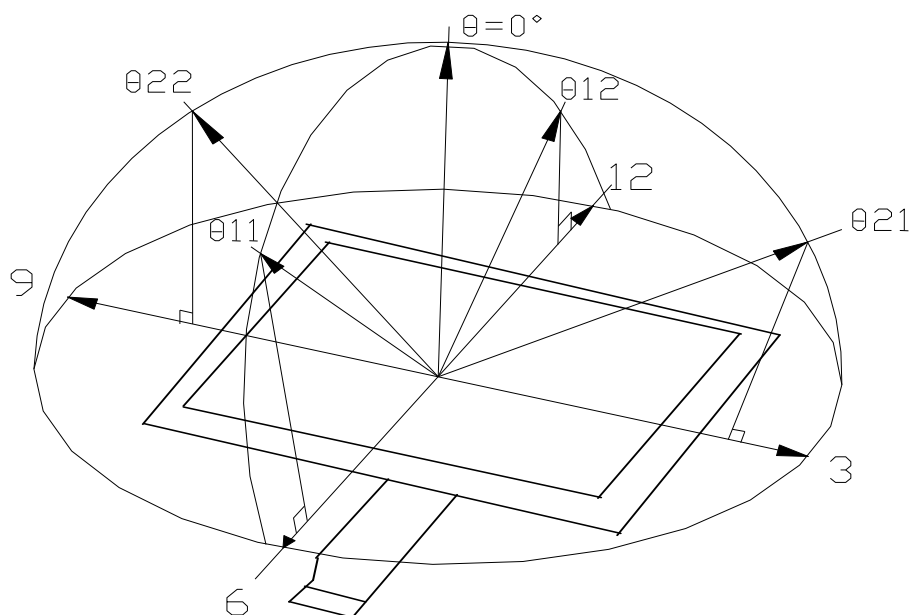
### 10-1) Specification

The backlight which PVI used is 5.6 inch for optical measuring and the specification of average brightness is  $4000(\text{cd}/\text{m}^2)$ .

$T_a = 25^\circ\text{C}$

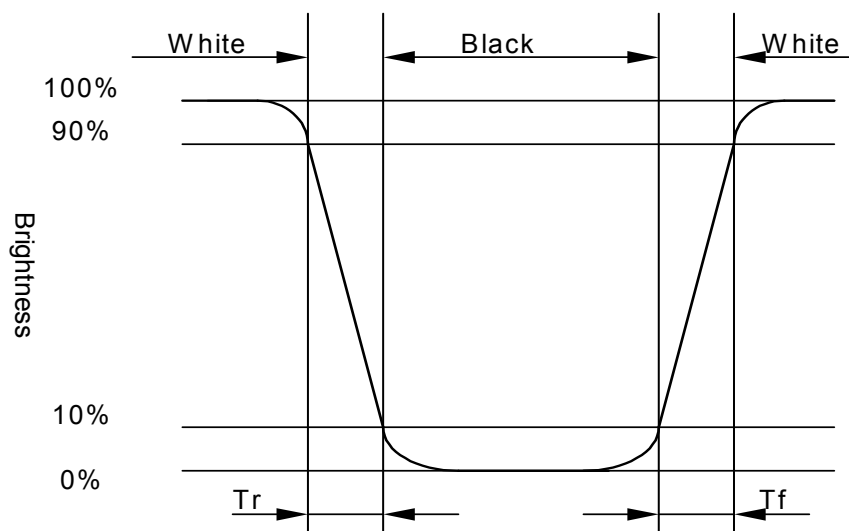
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	$\theta\ 21, \theta\ 22$	$CR \geq 10$	45	50	-	deg	Note 10-1
	Vertical	$\theta\ 12$		10	15	-	deg	
		$\theta\ 11$		30	35	-	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	350	-	-	Note 10-2
Transmission Ratio		T	$\theta = 0^{\circ}$	8.5	9.0	-	%	
Response time	Rise	Tr	$\theta = 0^{\circ}$	-	15	30	ms	Note 10-3
	Fall	Tf		-	25	50	ms	

**Note 10-1 : The definitions of viewing angles**

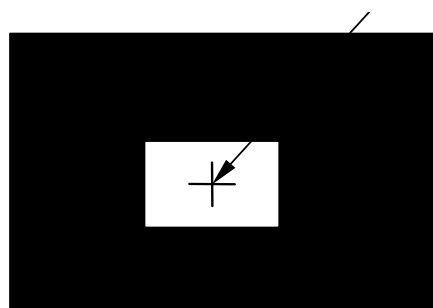
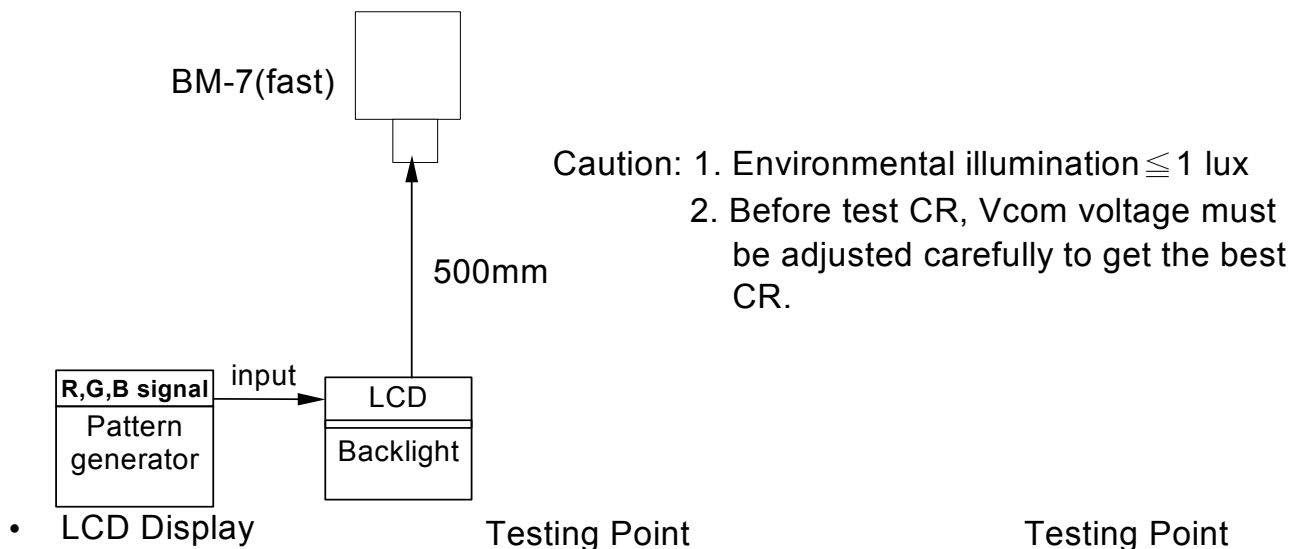


Note 10-2 :  $CR = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$   
 (Testing configuration see 10-2 )  
 Contrast Ratio is measured in optimum common electrode voltage.

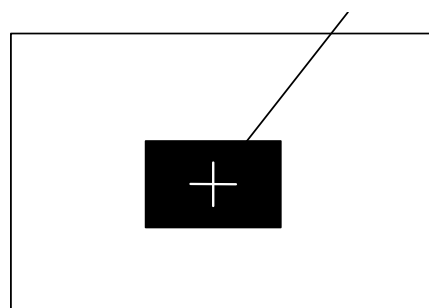
Note 10-3 : The definition of response time:



## 10-2) Testing configuration

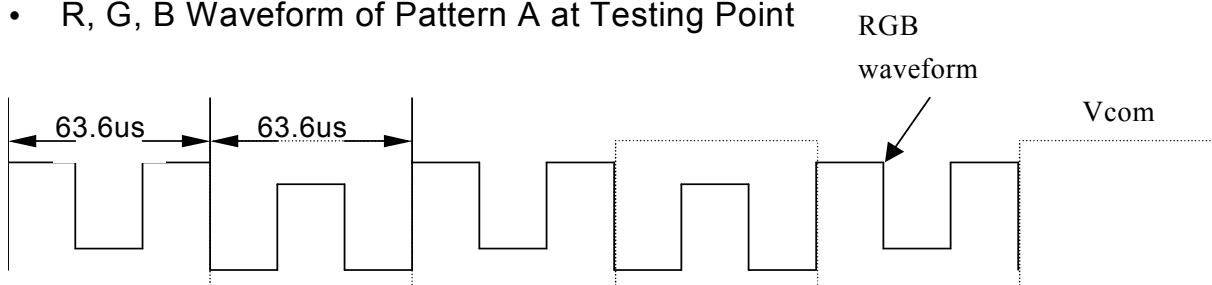


Pattern A

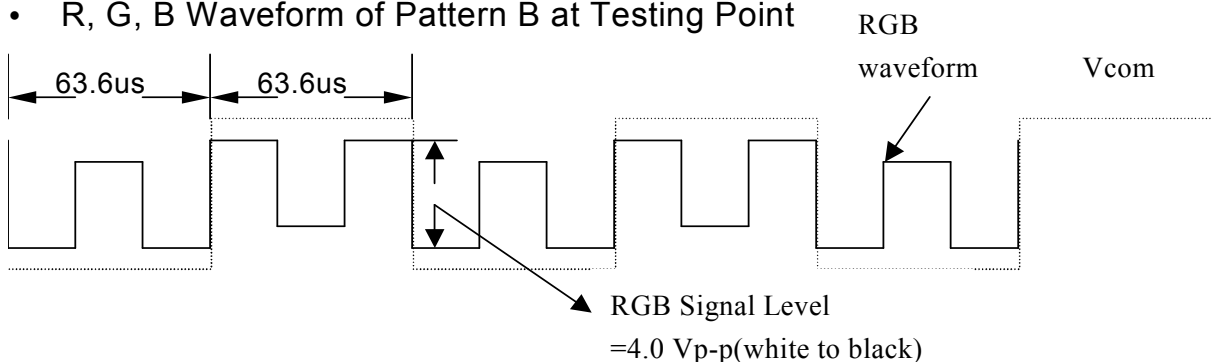


Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



## 11. Handling Cautions

### 11-1) Mounting of module

- Please power off the module when you connect the input/output connector.
- Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- Protective film (Laminator) is applied on surface to protect it against scratches and dirt.
- Please following the tear off direction as figure11-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

### 11-2) Precautions in mounting

- When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
- Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

### 11-3) Others

- Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- Store the module at a room temperature place.
- The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- Observe all other precautionary requirements in handling general electronic components.

### 11-4) Polarizer mark

The polarizer mark is to describe the direction of view angle film how to mach up with the rubbing direction.

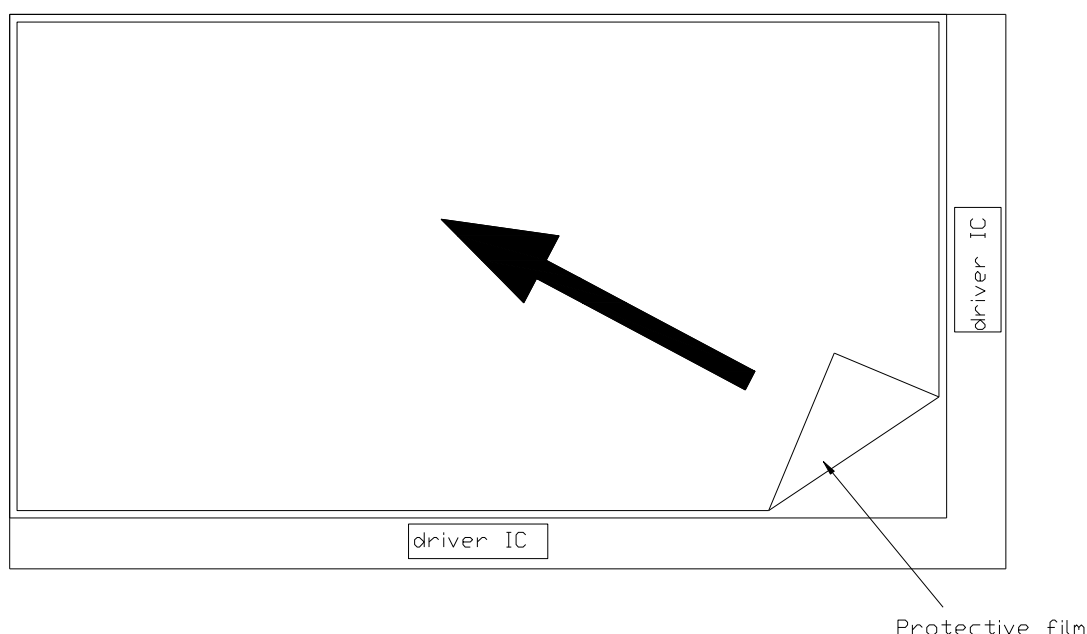


Figure 11-1 the way to peel off protective film

## 12. Reliability Test

No.	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70℃ , 240 hrs
2	Low Temperature Storage Test	Ta = -20℃ , 240 hrs
3	High Temperature Operation Test	Ta = +60℃ , 240 hrs
4	Low Temperature Operation Test	Ta = 0℃ , 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +50℃ , 80%RH , 240 hrs
6	Thermal Cycling Test (non-operating)	-20℃ → +70℃ , 200 Cycles 30 min 30 min
7	Electrostatic Discharge Test (non-operating)	200pF , 0Ω ±200V 1 time / each terminal

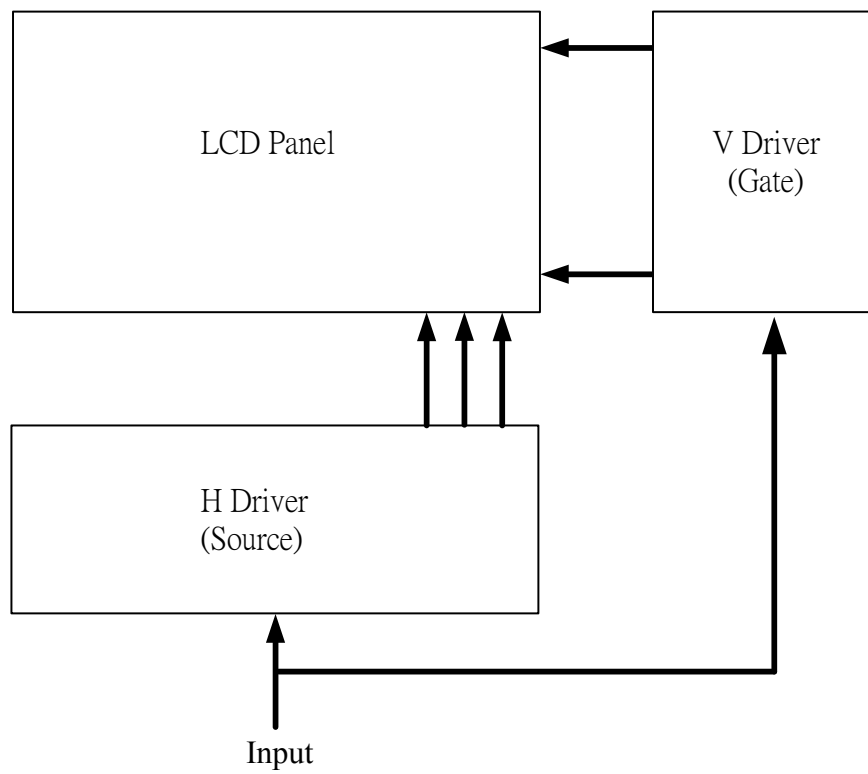
Ta: ambient temperature

Note : The protective film must be removed before temperature test.

### [Criteria]

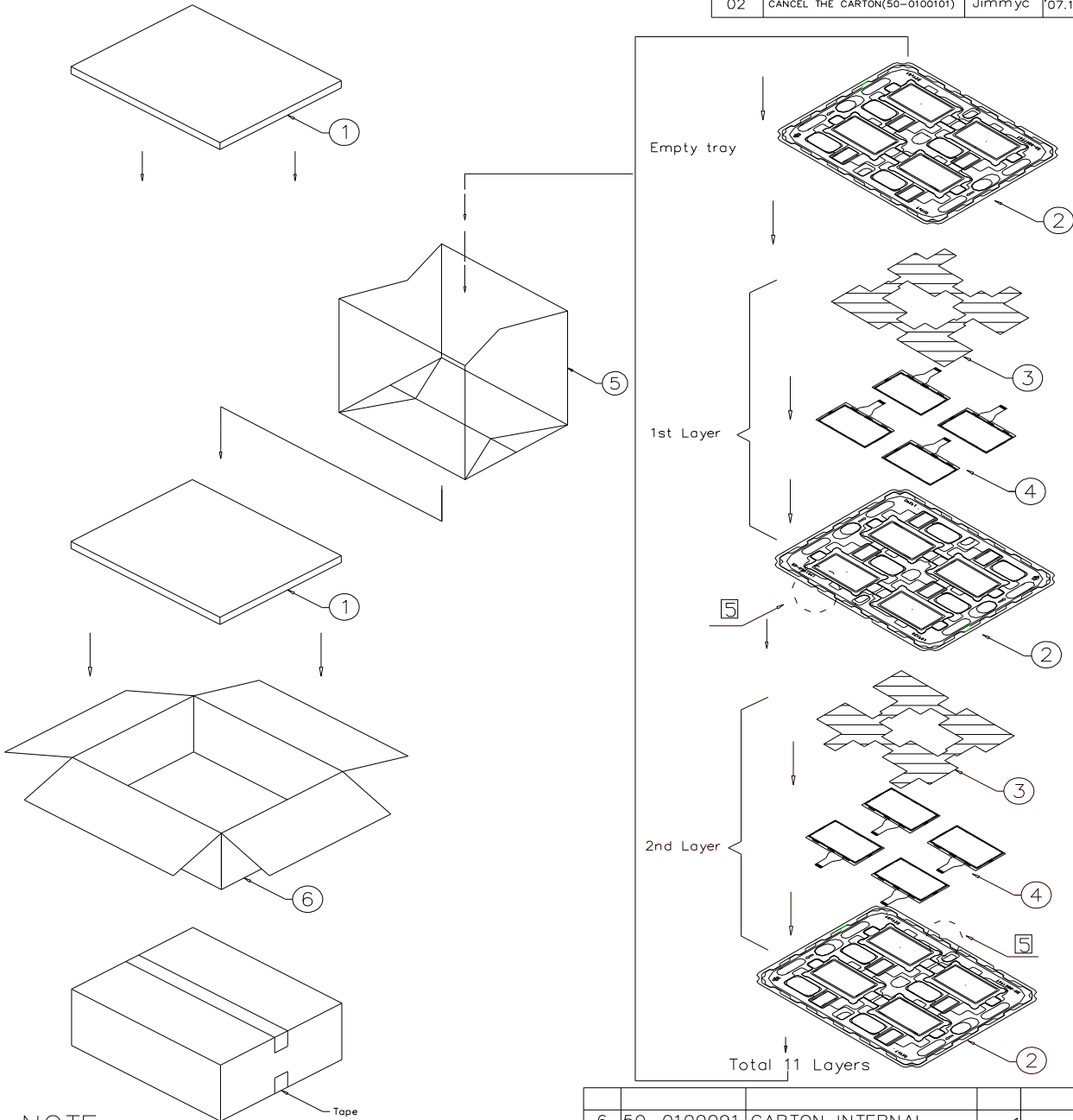
In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.

### 13. Block Diagram



## 14. Packing


REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	Jimmyc	07.05.23
02	CANCEL THE CARTON(50-0100101)	Jimmyc	07.11.05



**NOTE:**  
1. One layer include: 1 piece of cushion sheet, 4pcs panel & 1 piece of tray.  
2. Q'TY: 44 pcs panel/carton.  
3. Dimension: 455\*375\*190mm  
4. Weight: 4.2 KG  
5. tray 需180°交叉堆疊，疊堆後可從側邊檢視圓弧防呆方向是否正確

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
6	50-0100091	CARTON INTERNAL	1	
5	50-0500041	摺口袋450*380*700mm	1	抗靜電
4		PW056XU Panel	44	
3	50-0200057	EPE CUSHION SHEET	11	抗靜電
2	50-0301141	PS TRAY	12	抗靜電
1	50-0300491	EPE FOAM	2	

MTL.SPEC.		UNSPECIFIED TOL'S		REMARK	
		ANGLE			
		ROUGHNESS			
APPROVE	Frank Shin	SCALE	UNIT	SHEET	DWG.TITLE
CHECK	Frank Shin	1:1	mm	1 OF 1	PW056XU2 PACKING DRAW
DESIGN	Jimmyc	MTL.NO.		DWG.NO.	REV. 02
					A <sub>4</sub> SIZE

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Prime View International Co., Ltd.