

DATA SHEET

74LVC2G38

Dual 2-input NAND gate
(open drain)

Product specification
Supersedes data of 2003 Oct 27

2004 Oct 18

Dual 2-input NAND gate (open drain)

74LVC2G38

FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V).
- ESD protection:
 - HBM EIA/JESD22-A114-B exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V.
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Open drain outputs
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C.

DESCRIPTION

The 74LVC2G38 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. These feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off} . The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G38 provides the 2-input NAND function.

The outputs of the 74LVC2G38 devices are open drain and can be connected to other open-drain outputs to implement active-LOW, wired-OR or active-HIGH wired-AND functions.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|---|---|---------|------|
| t_{PZL}/t_{PLZ} | propagation delay inputs nA and nB to output nY | $V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k Ω | 3.0 | ns |
| | | $V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ Ω | 1.8 | ns |
| | | $V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ Ω | 2.5 | ns |
| | | $V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ Ω | 2.1 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ Ω | 1.5 | ns |
| C_I | input capacitance | | 2.5 | pF |
| C_{PD} | power dissipation capacitance per gate | $V_{CC} = 3.3$ V; notes 1 and 2 | 5 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. The condition is $V_I = \text{GND}$ to V_{CC} .

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FUNCTION TABLE

See note 1.

| INPUT | | OUTPUT |
|-------|----|--------|
| nA | nB | nY |
| L | L | Z |
| L | H | Z |
| H | L | Z |
| H | H | L |

Note

1. H = HIGH voltage level;
 L = LOW voltage level;
 Z = high-impedance OFF-state.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | | | |
|-------------|-------------------|------|---------|----------|----------|---------|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE | MARKING |
| 74LVC2G38DP | −40 °C to +125 °C | 8 | TSSOP8 | plastic | SOT505-2 | Y38 |
| 74LVC2G38DC | −40 °C to +125 °C | 8 | VSSOP8 | plastic | SOT765-1 | Y38 |
| 74LVC2G38GM | −40 °C to +125 °C | 8 | XSON8 | plastic | SOT833-1 | Y38 |

PINNING

| PIN | SYMBOL | DESCRIPTION |
|-----|-----------------|----------------|
| 1 | 1A | data input |
| 2 | 1B | data input |
| 3 | 2Y | data output |
| 4 | GND | ground (0 V) |
| 5 | 2A | data input |
| 6 | 2B | data input |
| 7 | 1Y | data output |
| 8 | V _{CC} | supply voltage |

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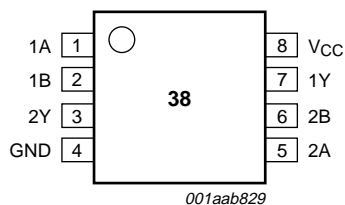


Fig.1 Pin configuration TSSOP8 and VSSOP8.

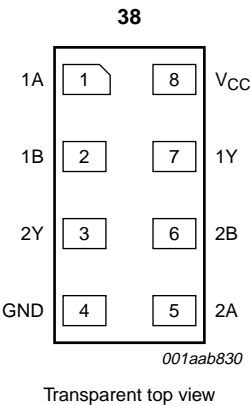


Fig.2 Pin configuration XSON8.

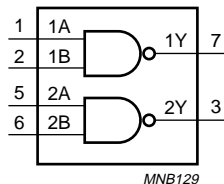


Fig.3 Logic symbol.

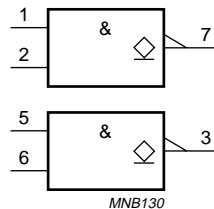


Fig.4 Logic symbol (IEEE/IEC).

Dual 2-input NAND gate (open drain)

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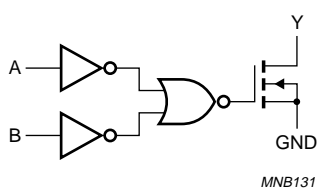


Fig.5 Logic diagram (one gate).

Dual 2-input NAND gate (open drain)

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------|-------------------------------|---|------|----------|------|
| V_{CC} | supply voltage | | 1.65 | 5.5 | V |
| V_I | input voltage | | 0 | 5.5 | V |
| V_O | output voltage | active mode | 0 | V_{CC} | V |
| | | $V_{CC} = 1.65\text{ V to }5.5\text{ V}$; disable mode | 0 | 5.5 | V |
| | | $V_{CC} = 0\text{ V}$; Power-down mode | 0 | 5.5 | V |
| T_{amb} | operating ambient temperature | | -40 | +125 | °C |
| t_r, t_f | input rise and fall times | $V_{CC} = 1.65\text{ V to }2.7\text{ V}$ | 0 | 20 | ns/V |
| | | $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ | 0 | 10 | ns/V |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-------------------|-------------------------------|---|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input diode current | $V_I < 0\text{ V}$ | - | -50 | mA |
| V_I | input voltage | note 1 | -0.5 | +6.5 | V |
| I_{OK} | output diode current | $V_O > V_{CC}$ or $V_O < 0\text{ V}$ | - | ±50 | mA |
| V_O | output voltage | active mode; notes 1 and 2 | -0.5 | +6.5 | V |
| | | Power-down mode; notes 1 and 2 | -0.5 | +6.5 | V |
| I_O | output source or sink current | $V_O = 0\text{ V to }V_{CC}$ | - | ±50 | mA |
| I_{CC}, I_{GND} | V_{CC} or GND current | | - | ±100 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_D | power dissipation | $T_{amb} = -40\text{ °C to }+125\text{ °C}$ | - | 300 | mW |

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When $V_{CC} = 0\text{ V}$ (Power-down mode), the output voltage can be 5.5 V in normal operation.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---------------------|------------------------|------|------------------------|------|
| | | OTHER | V _{CC} (V) | | | | |
| T _{amb} = −40 °C to +85 °C; note 1 | | | | | | | |
| V _{IH} | HIGH-level input voltage | | 1.65 to 1.95 | 0.65 × V _{CC} | – | – | V |
| | | | 2.3 to 2.7 | 1.7 | – | – | V |
| | | | 2.7 to 3.6 | 2.0 | – | – | V |
| | | | 4.5 to 5.5 | 0.7 × V _{CC} | – | – | V |
| V _{IL} | LOW-level input voltage | | 1.65 to 1.95 | – | – | 0.35 × V _{CC} | V |
| | | | 2.3 to 2.7 | – | – | 0.7 | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | V |
| | | | 4.5 to 5.5 | – | – | 0.3 × V _{CC} | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | |
| | | I _O = 100 μA | 1.65 to 5.5 | – | – | 0.1 | V |
| | | I _O = 4 mA | 1.65 | – | 0.08 | 0.45 | V |
| | | I _O = 8 mA | 2.3 | – | 0.14 | 0.3 | V |
| | | I _O = 12 mA | 2.7 | – | 0.19 | 0.4 | V |
| | | I _O = 24 mA | 3.0 | – | 0.37 | 0.55 | V |
| | | I _O = 32 mA | 4.5 | – | 0.43 | 0.55 | V |
| I _{LI} | input leakage current | V _I = 5.5 V or GND | 5.5 | – | ±0.1 | ±5 | μA |
| I _{off} | power OFF leakage current | V _I or V _O = 5.5 V | 0 | – | ±0.1 | ±10 | μA |
| I _{CC} | quiescent supply current | V _I = V _{CC} or GND; I _O = 0 A | 5.5 | – | 0.1 | 10 | μA |
| ΔI _{CC} | additional quiescent supply current per pin | V _I = V _{CC} – 0.6 V; I _O = 0 A | 2.3 to 5.5 | – | 5 | 500 | μA |

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| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|--------------------------------------|---|---|---------------------|------------------------|------|------------------------|------|
| | | OTHER | V _{CC} (V) | | | | |
| T _{amb} = −40 °C to +125 °C | | | | | | | |
| V _{IH} | HIGH-level input voltage | | 1.65 to 1.95 | 0.65 × V _{CC} | — | — | V |
| | | | 2.3 to 2.7 | 1.7 | — | — | V |
| | | | 2.7 to 3.6 | 2.0 | — | — | V |
| | | | 4.5 to 5.5 | 0.7 × V _{CC} | — | — | V |
| V _{IL} | LOW-level input voltage | | 1.65 to 1.95 | — | — | 0.35 × V _{CC} | V |
| | | | 2.3 to 2.7 | — | — | 0.7 | V |
| | | | 2.7 to 3.6 | — | — | 0.8 | V |
| | | | 4.5 to 5.5 | — | — | 0.3 × V _{CC} | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | |
| | | I _O = 100 μA | 1.65 to 5.5 | — | — | 0.1 | V |
| | | I _O = 4 mA | 1.65 | — | — | 0.70 | V |
| | | I _O = 8 mA | 2.3 | — | — | 0.45 | V |
| | | I _O = 12 mA | 2.7 | — | — | 0.60 | V |
| | | I _O = 24 mA | 3.0 | — | — | 0.80 | V |
| | | I _O = 32 mA | 4.5 | — | — | 0.80 | V |
| I _{LI} | input leakage current | V _I = 5.5 V or GND | 5.5 | — | — | ±20 | μA |
| I _{off} | power OFF leakage current | V _I or V _O = 5.5 V | 0 | — | — | ±20 | μA |
| I _{CC} | quiescent supply current | V _I = V _{CC} or GND; I _O = 0 A | 5.5 | — | — | 40 | μA |
| ΔI _{CC} | additional quiescent supply current per pin | V _I = V _{CC} − 0.6 V; I _O = 0 A | 2.3 to 5.5 | — | — | 5000 | μA |

Note

1. All typical values are measured at T_{amb} = 25 °C.

Dual 2-input NAND gate (open drain)

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AC CHARACTERISTICS

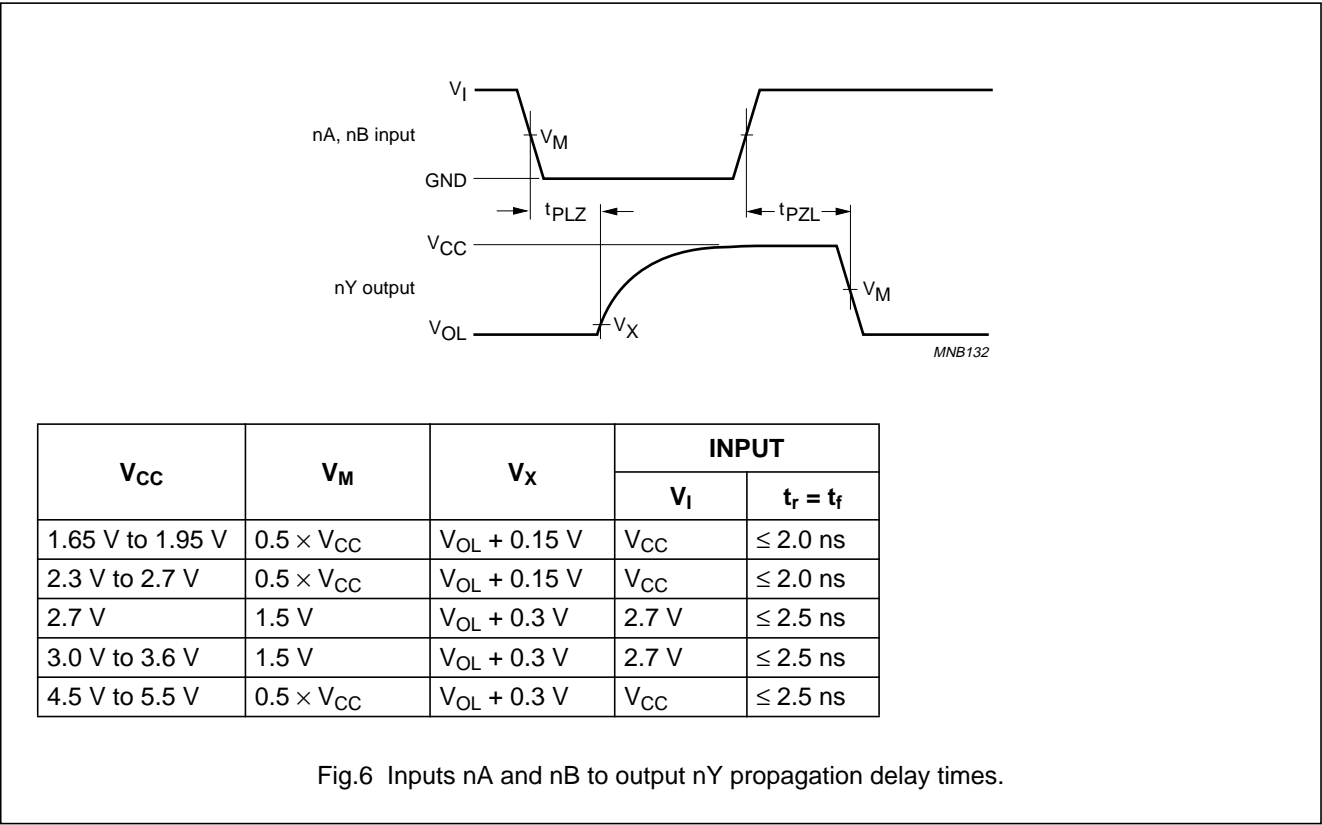
GND = 0 V.

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|------------------|---------------------|------|------|------|------|
| | | WAVEFORMS | V _{CC} (V) | | | | |
| T _{amb} = −40 °C to +85 °C; note 1 | | | | | | | |
| t _{PZL} /t _{PLZ} | propagation delay inputs nA and nB to output nY | see Figs 6 and 7 | 1.65 to 1.95 | 1.2 | 3.0 | 8.6 | ns |
| | | | 2.3 to 2.7 | 0.7 | 1.8 | 4.8 | ns |
| | | | 2.7 | 0.7 | 2.5 | 4.4 | ns |
| | | | 3.0 to 3.6 | 0.7 | 2.1 | 4.1 | ns |
| | | | 4.5 to 5.5 | 0.5 | 1.5 | 3.3 | ns |
| T _{amb} = −40 °C to +125 °C | | | | | | | |
| t _{PZL} /t _{PLZ} | propagation delay inputs nA and nB to output nY | see Figs 6 and 7 | 1.65 to 1.95 | 1.2 | — | 10.8 | ns |
| | | | 2.3 to 2.7 | 0.7 | — | 6.0 | ns |
| | | | 2.7 | 0.7 | — | 5.5 | ns |
| | | | 3.0 to 3.6 | 0.7 | — | 5.2 | ns |
| | | | 4.5 to 5.5 | 0.5 | — | 4.2 | ns |

Note

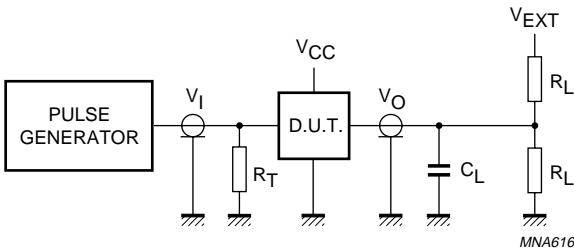
1. All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS



Dual 2-input NAND gate (open drain)

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| V _{CC} | V _I | C _L | R _L | V _{EXT} | | |
|------------------|-----------------|----------------|----------------|------------------------------------|------------------------------------|------------------------------------|
| | | | | t _{PLH} /t _{PHL} | t _{PZH} /t _{PHZ} | t _{PZL} /t _{PLZ} |
| 1.65 V to 1.95 V | V _{CC} | 30 pF | 1 kΩ | open | GND | 2 × V _{CC} |
| 2.3 V to 2.7 V | V _{CC} | 30 pF | 500 Ω | open | GND | 2 × V _{CC} |
| 2.7 V | 2.7 V | 50 pF | 500 Ω | open | GND | 6 V |
| 3.0 V to 3.6 V | 2.7 V | 50 pF | 500 Ω | open | GND | 6 V |
| 4.5 V to 5.5 V | V _{CC} | 50 pF | 500 Ω | open | GND | 2 × V _{CC} |

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

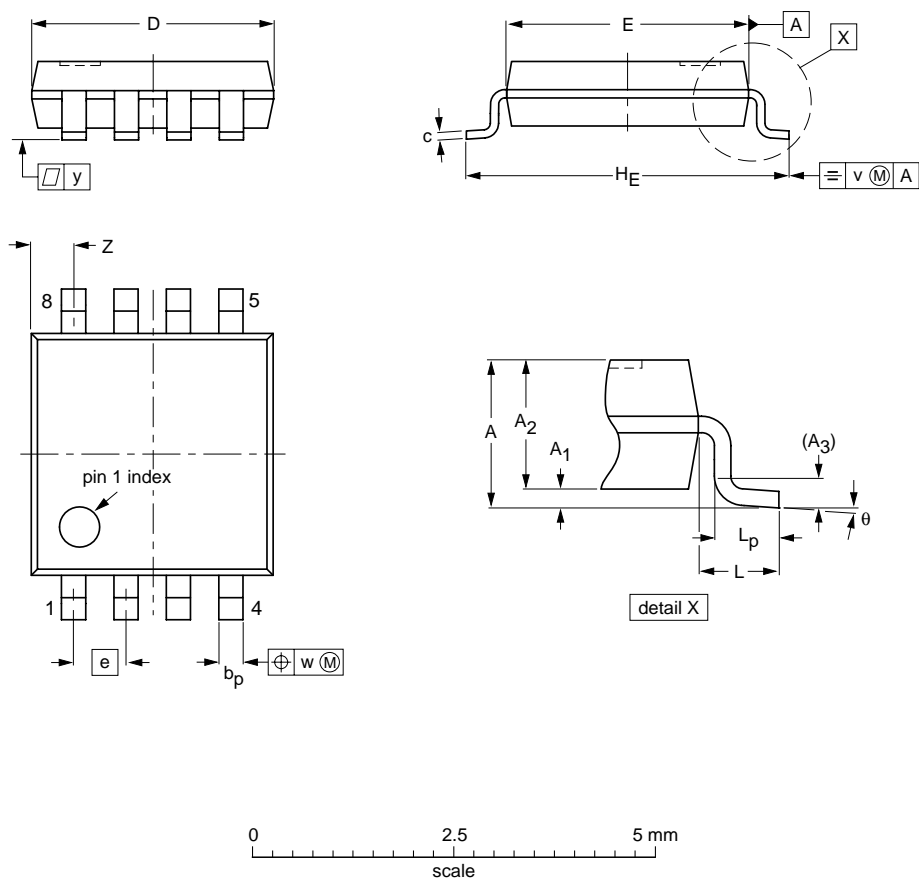
Fig.7 Load circuitry for switching times.

Dual 2-input NAND gate (open drain)

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PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

| UNIT | A _{max.} | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | v | w | y | z ⁽¹⁾ | θ |
|------|-------------------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|-----|----------------|-----|------|-----|------------------|----------|
| mm | 1.1 | 0.15 0.00 | 0.95 0.75 | 0.25 | 0.38 0.22 | 0.18 0.08 | 3.1 2.9 | 3.1 2.9 | 0.65 | 4.1 3.9 | 0.5 | 0.47 0.33 | 0.2 | 0.13 | 0.1 | 0.70 0.35 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

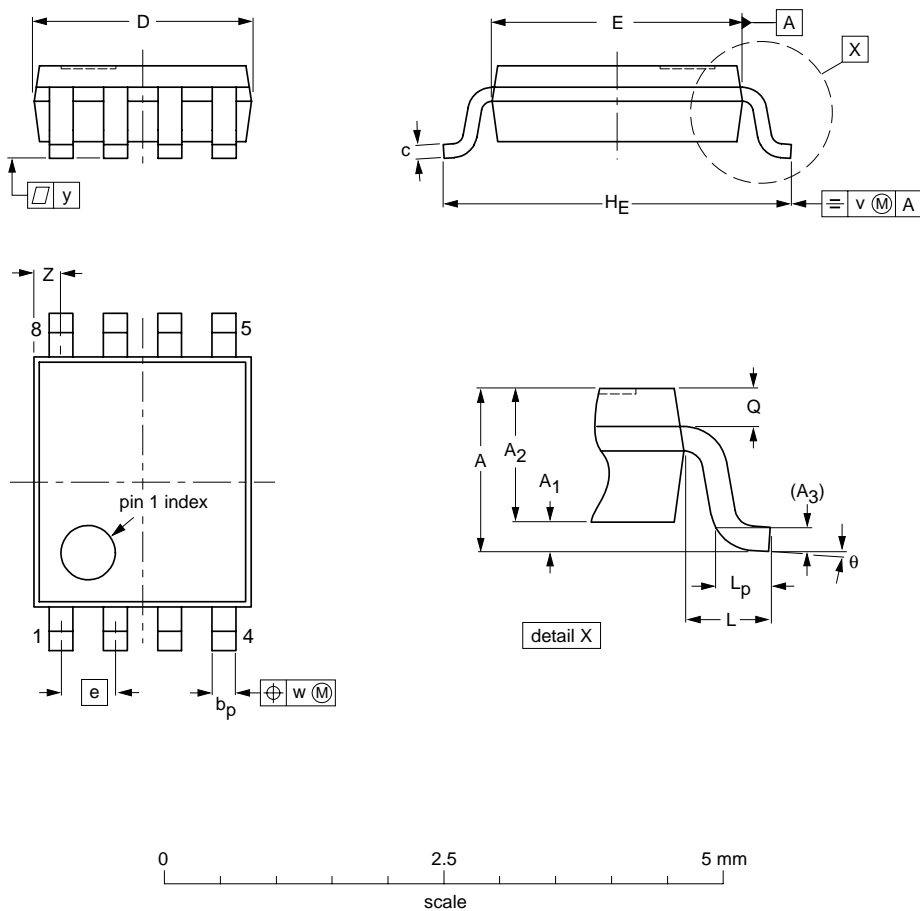
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|-------|--|------------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT505-2 | | --- | | | | 02-01-16 |

Dual 2-input NAND gate (open drain)

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VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|------|-----------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|-----|----------------|--------------|-----|------|-----|------------------|----------|
| mm | 1 | 0.15 0.00 | 0.85 0.60 | 0.12 | 0.27 0.17 | 0.23 0.08 | 2.1 1.9 | 2.4 2.2 | 0.5 | 3.2 3.0 | 0.4 | 0.40 0.15 | 0.21 0.19 | 0.2 | 0.13 | 0.1 | 0.4 0.1 | 8° 0° |

- Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

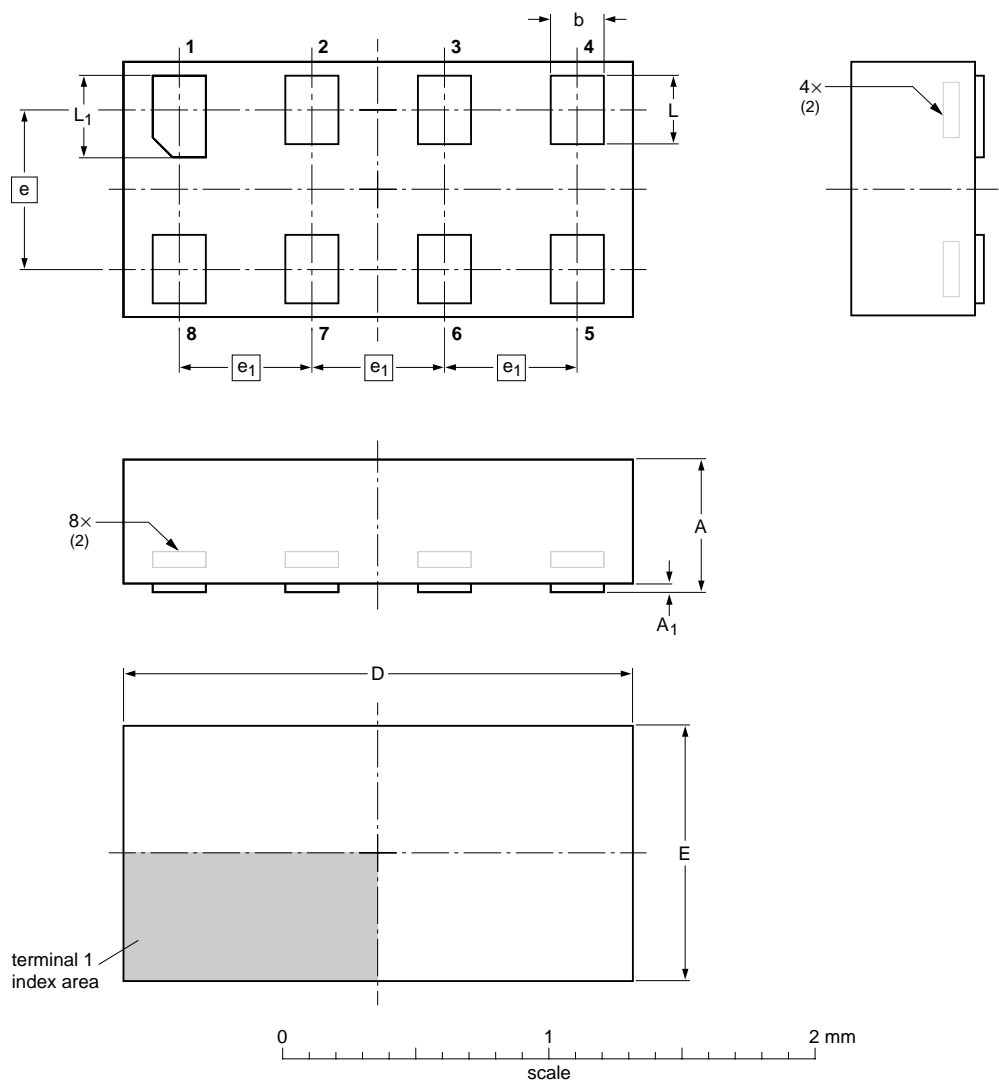
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|--------|-------|--|------------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT765-1 | | MO-187 | | | | 02-06-07 |

Dual 2-input NAND gate (open drain)

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XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 0.95 x 1.95 x 0.5 mm


SOT833-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A ⁽¹⁾ max | A ₁ max | b | D | E | e | e ₁ | L | L ₁ |
|------|-------------------------|-----------------------|--------------|------------|------------|-----|----------------|--------------|----------------|
| mm | 0.5 | 0.04 | 0.25 0.17 | 2.0 1.9 | 1.0 0.9 | 0.6 | 0.5 | 0.35 0.27 | 0.40 0.32 |

- Notes**
1. Including plating thickness.
 2. Can be visible in some manufacturing processes.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|--------|-------|--|---|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT833-1 | --- | MO-252 | --- | |  | 04-07-15 04-07-22 |

Dual 2-input NAND gate (open drain)

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DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾⁽³⁾ | DEFINITION |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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Notes

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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