

Low Power Current Mode Push-Pull PWM

FEATURES

- 130µA Typical Starting Current
- 1mA Typical Run Current
- Operation to 1MHz
- Internal Soft Start
- On Chip Error Amplifier With 2MHz Gain Bandwidth Product
- On Chip VDD Clamping
- Dual Output Drive Stages In Push-Pull Configuration
- Output Drive Stages Capable Of 500mA Peak Source Current, 1A Peak Sink Current

DESCRIPTION

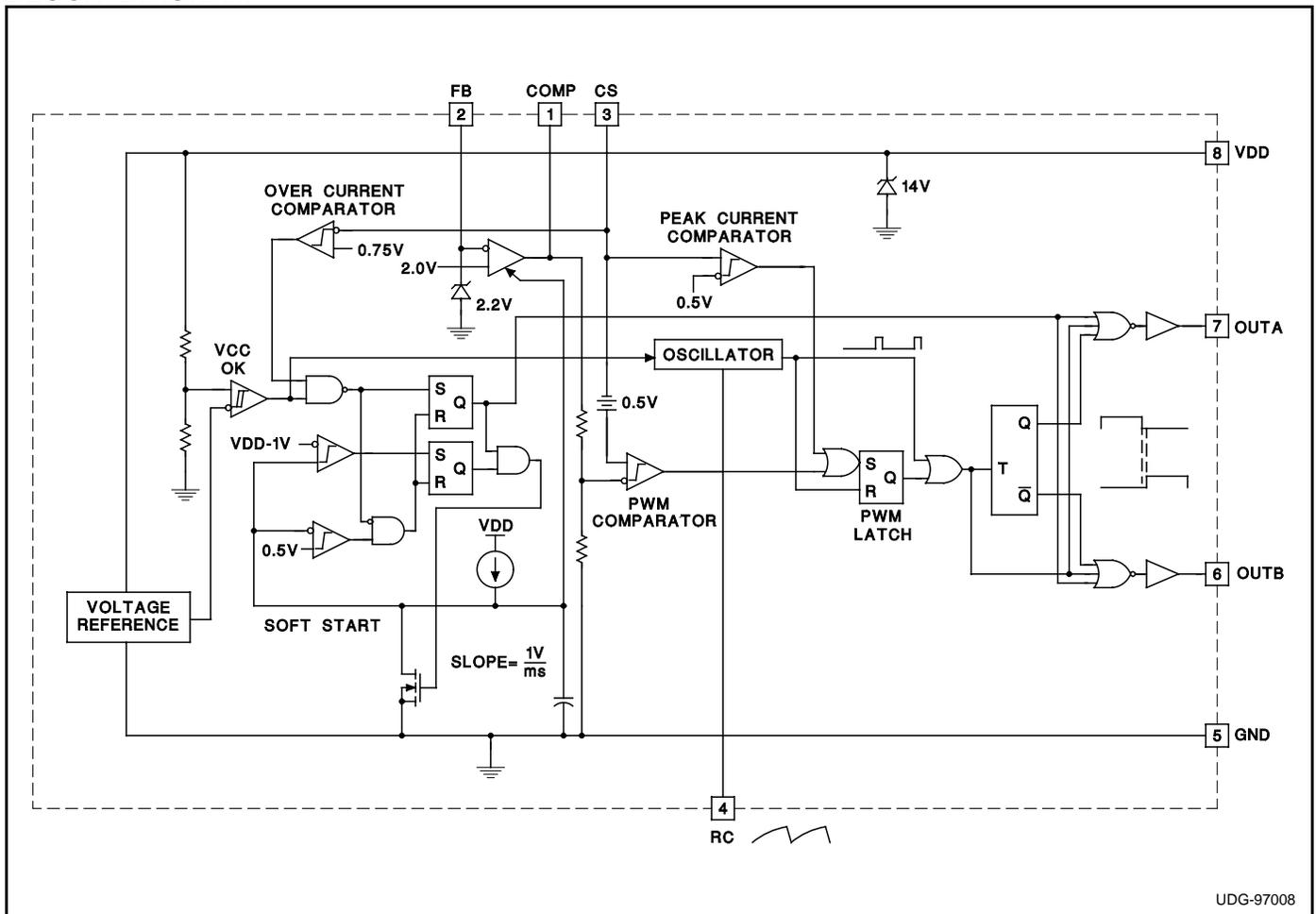
The UCC3808 is a family of BiCMOS push-pull, high-speed, low power, pulse width modulators. The UCC3808 contains all of the control and drive circuitry required for off-line or DC-to-DC fixed frequency current-mode switching power supplies with minimal external parts count.

The UCC3808 dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60ns to 200ns depending on the values of the timing capacitor and resistors, thus limits each output stage duty cycle to less than 50%.

The UCC3808 family offers a variety of package options temperature range options, and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for off-line and battery powered systems. Thresholds are shown in the table below.

| Part Number | Turn on Threshold | Turn off Threshold |
|-------------|-------------------|--------------------|
| UCCx808-1 | 12.5V | 8.3V |
| UCCx808-2 | 4.3V | 4.1V |

BLOCK DIAGRAM

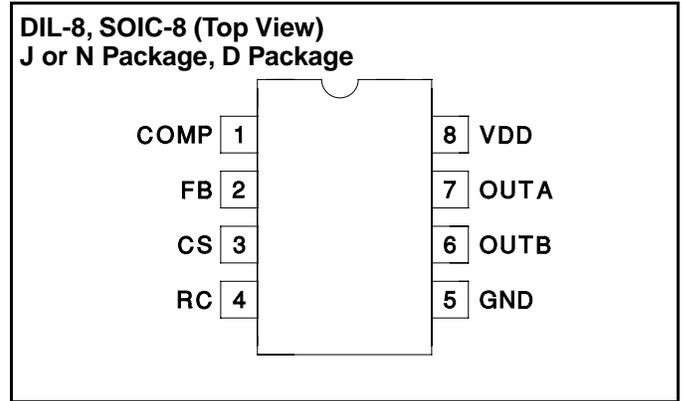


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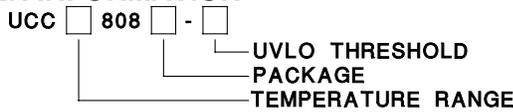
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($I_{DD} \leq 10\text{mA}$) 15V
 Supply Current 20mA
 OUTA/OUTB Source Current (peak) -500mA
 OUTA/OUTB Sink Current (peak) 1000mA
 Analog Inputs (FB, CS) -0.3V to $V_{DD}+0.3\text{V}$, not to exceed 6V
 Power Dissipation at $T_A = 25^\circ\text{C}$ (N Package) 1W
 Power Dissipation at $T_A = 25^\circ\text{C}$ (D Package) 650mW
 Storage Temperature -65°C to $+150^\circ\text{C}$
 Junction Temperature -55°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10sec.) $+300^\circ\text{C}$
*Currents are positive into, negative out of the specified terminal.
 Consult Packaging Section of Databook for thermal limitations
 and considerations of package.*

CONNECTION DIAGRAM



ORDER INFORMATION



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, $T_A = 0^\circ\text{C}$ to 70°C for UCC3808-X, -40°C to 85°C for UCC2808-X and -55°C to 125°C UCC1808-X, $V_{DD} = 10\text{V}$ (Note 6), $1\mu\text{F}$ capacitor from V_{DD} to GND , Oscillator $R = 22\text{k}\Omega$, $C = 330\text{pF}$. $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|--|------|------|------|---------------|
| Oscillator Section | | | | | |
| Oscillator Frequency | | 175 | 194 | 213 | kHz |
| Oscillator Amplitude/ V_{DD} | (Note 1) | 0.44 | 0.5 | 0.56 | V/V |
| Error Amplifier Section | | | | | |
| Input Voltage | COMP = 2V | 1.95 | 2 | 2.05 | V |
| Input Bias Current | | -1 | | 1 | μA |
| Open Loop Voltage Gain | | 60 | 80 | | dB |
| COMP Sink Current | FB = 2.2V, COMP = 1V | 0.3 | 2.5 | | mA |
| COMP Source Current | FB = 1.3V, COMP = 3.5V | -0.2 | -0.5 | | mA |
| PWM Section | | | | | |
| Maximum Duty Cycle | Measured at OUTA or OUTB | 48 | 49 | 50 | % |
| Minimum Duty Cycle | COMP = 0V | | | 0 | % |
| Current Sense Section | | | | | |
| Gain | (Note 2) | 1.3 | 1.5 | 1.7 | V/V |
| Maximum Input Signal | COMP = 5V (Note 3) | 0.45 | 0.5 | 0.55 | V |
| CS to Output Delay | COMP = 3.5V, CS from 0 to 600mV | | 100 | 200 | ns |
| Input Bias Current | | -200 | | 200 | nA |
| Over Current Threshold | | 0.7 | 0.75 | 0.8 | V |
| COMP to CS Offset | CS = 0V | 0.4 | 0.7 | 1 | V |
| Output Section | | | | | |
| OUT Low Level | $I = 100\text{mA}$ | | 0.5 | 1 | V |
| OUT High Level | $I = -50\text{mA}$, $V_{DD} - \text{OUT}$ | | 0.5 | 1 | V |
| Rise Time | $C_L = 1\text{nF}$ | | 40 | 120 | ns |
| Fall Time | $C_L = 1\text{nF}$ | | 20 | 60 | ns |
| Undervoltage Lockout Section | | | | | |
| Start Threshold | UCCx808-1 (Note 4) | 11.5 | 12.5 | 13.5 | V |
| | UCCx808-2 | 4.1 | 4.3 | 4.5 | V |
| Minimum Operating Voltage After Start | UCCx808-1 (Note 4) | 7.6 | 8.3 | 9 | V |
| | UCCx808-2 | 3.9 | 4.1 | 4.3 | V |
| Hysteresis | UCCx808-1 | 3.5 | 4.2 | 5.1 | V |
| | UCCx808-2 | 0.1 | 0.2 | 0.3 | V |

ELECTRICAL CHARACTERISTICS (cont): Unless otherwise specified, $T_A = 0^\circ\text{C}$ to 70°C for UCC3808-X, -40°C to 85°C for UCC2808-X and -55°C to 125°C UCC1808-X, $V_{DD} = 10\text{V}$ (Note 6), $1\mu\text{F}$ capacitor from V_{DD} to GND , Oscillator $R = 22\text{k}\Omega$, $C = 330\text{pF}$. $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|-----------------------------------|-----|-----|-----|---------------|
| Soft Start Section | | | | | |
| COMP Rise Time | FB = 1.8V, Rise from 0.5V to 4V | | 3.5 | | ms |
| Overall Section | | | | | |
| Startup Current | $V_{DD} < \text{Start Threshold}$ | | 130 | 260 | μA |
| Operating Supply Current | FB = 0V, CS = 0V (Note 5 and 6) | | 1 | 2 | mA |
| VDD Zener Shunt Voltage | IDD = 10mA | 13 | 14 | 15 | V |

Note 1: Measured at RC. Signal amplitude tracks VDD.

Note 2: Gain is defined by

$$A = \frac{\Delta V_{\text{COMP}}}{\Delta V_{\text{CS}}}, 0 \leq V_{\text{CS}} \leq 0.4\text{V}.$$

Note 3: Parameter measured at trip point of latch with FB at 0V.

Note 4: Start threshold and Zener Shunt threshold track one another.

Note 5: Does not include current in the external oscillator network.

Note 6: For UCCx808-1, set VDD above the start threshold before setting at 10V.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3808 is a true low-output impedance, 2MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC3808 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: The input to the PWM and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold will cause a soft start cycle.

FB: The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: Reference ground and power ground for all functions. Due to high currents, and high frequency operation of the UCC3808, a low impedance circuit board ground plane is highly recommended.

OUTA and OUTB: Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500mA peak source current, and 1A peak sink current.

The output stages switch at half the oscillator frequency, in a push/pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This "dead time" between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60ns to 200ns and

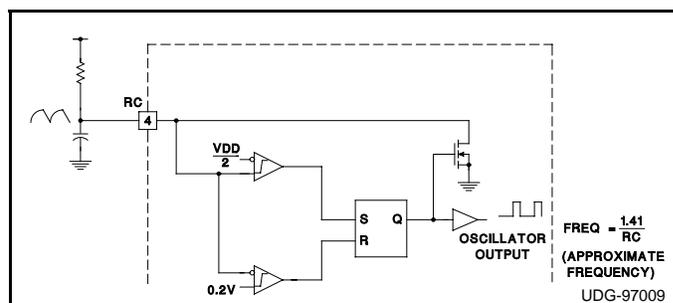
is depended upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which can switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

RC: The oscillator programming pin. The UCC3808's oscillator tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Figure 1 shows the oscillator block diagram.

Only two components are required to program the oscillator, a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula

$$f_{\text{OSCILLATOR}} = \frac{1.41}{RC}$$



The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time.

The output stages switch at 1/2 the oscillator frequency, with guaranteed duty cycle of < 50% for both outputs.

Figure 1. Block Diagram for Oscillator

